MS-7678

uATX Ver: 1.0

CPU:

INTEL - Sandy Bridge LGA 1155

System Chipset:

INTEL - Cougar Point PCH

OnBoard Chipset:

Clock Gen:IDT 4105
HD Audio Codec:RTL892
LAN:RTL 8111E 10/100/1000
SIO:FIN71889ED
Flash ROM: 32 Mb SPI (PCH)

Main Memory:

DDRIII (1066/1333MHz) * 4 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 3

PWM:

Controller:VRD12 ISL6364CRZ 4+1-Phase

CPU+GPU
Controller:uP6138
CPU VTT CPU SA
Controller:uP6138
DDR PCH

ACPI:

UPI

Other:

SATA3.0 x2 + SATA2.0 x4 (PCH)
SATA3.0X1 + e-SATA X1(MARVELL9128_COLAY_E9172)
USB2.0 RearX4 Front x8(PCH&BC Charge & i Charge)
USB3.0 RearX2 (NEC USB3.0)
1394 Controller - VT6315N-CE
D-SUB *1
DVI-D PORT*1
HDMI *1
TPM Header *1
COM Header *1
on BOARD BUZZER

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Manual & Option
Manual & Option
Manual & Option

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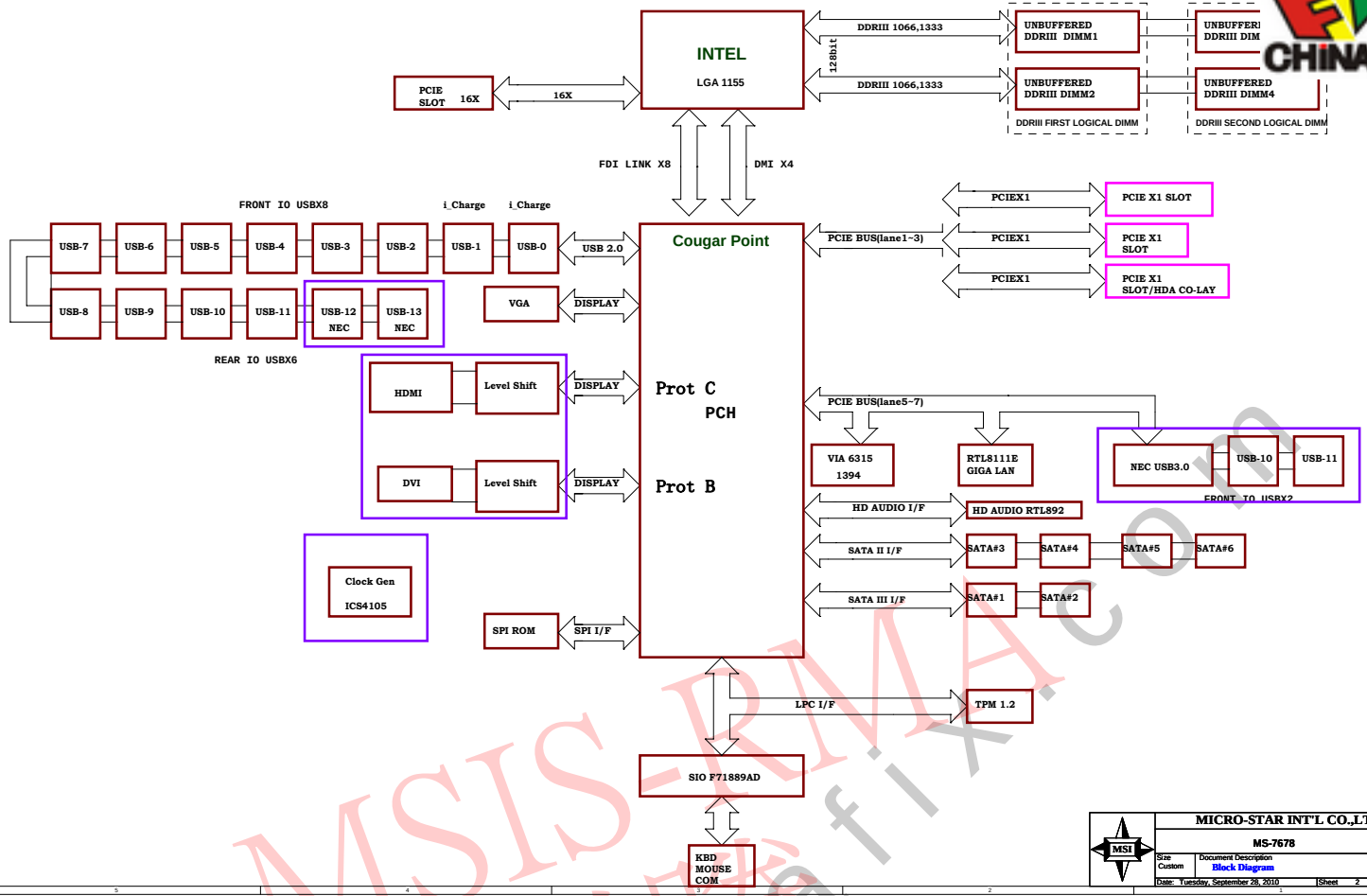

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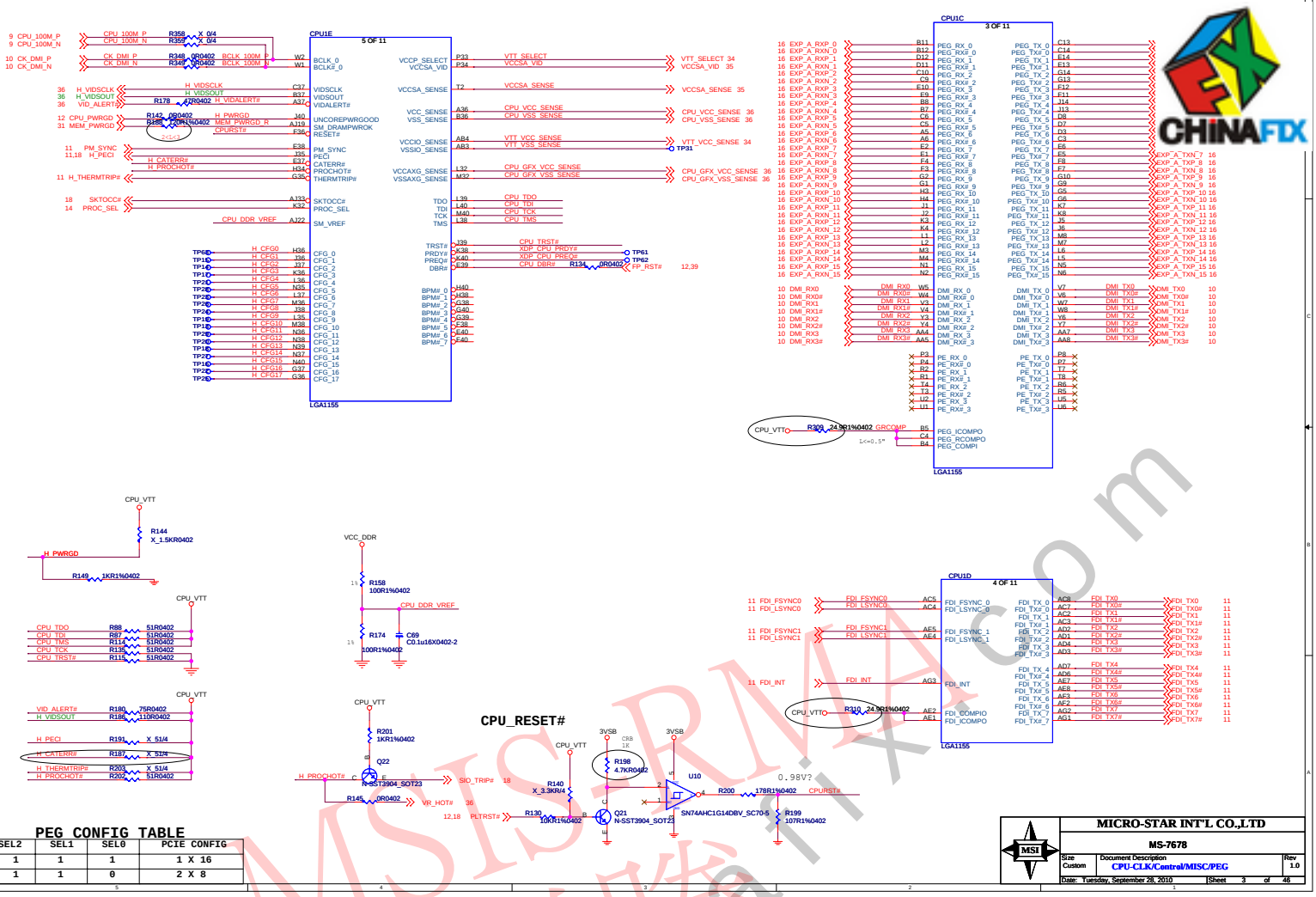

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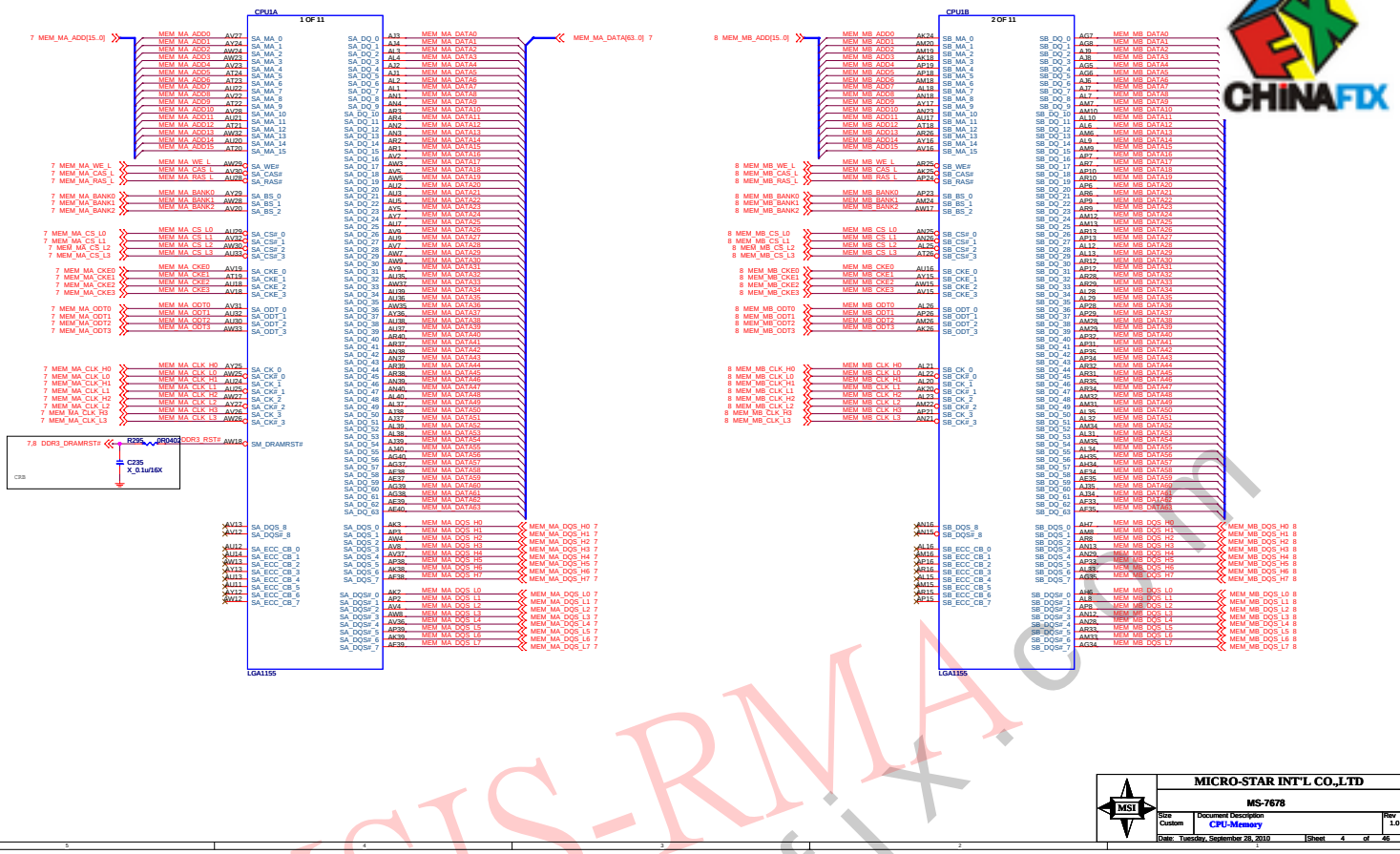

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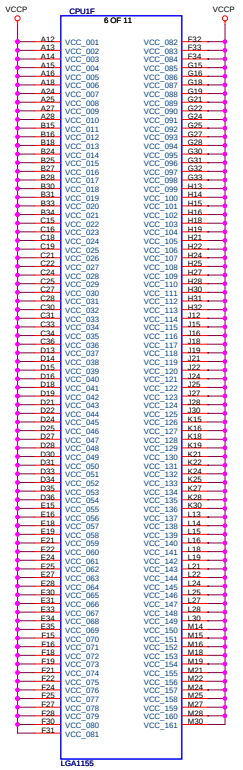
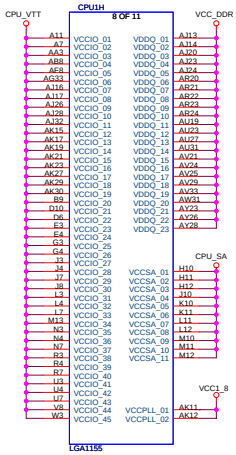
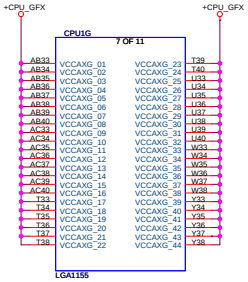
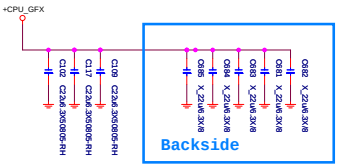






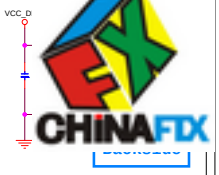
VCCP: 112A
CPU_VTT: 8.2A
CPU_SA: 8.8A
VCC_DDR: 25A
VCC1_8: 1.6A

+CPU_GFX Decoupling

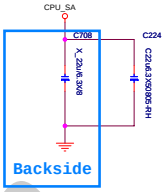


CPU SOCKET CAVITY CAPS

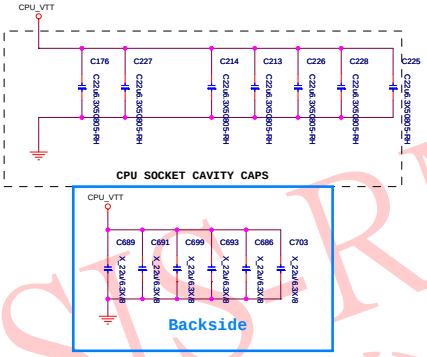
+1.5V_DDR3-Decoupling



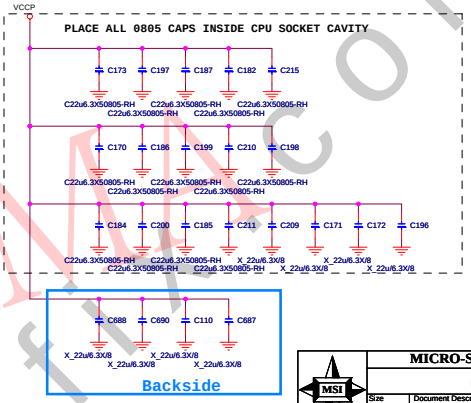
CPU SOCKET CAVITY CAPS

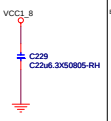


+CPU_VTT Decoupling



+CPU_VCCP-Decoupling





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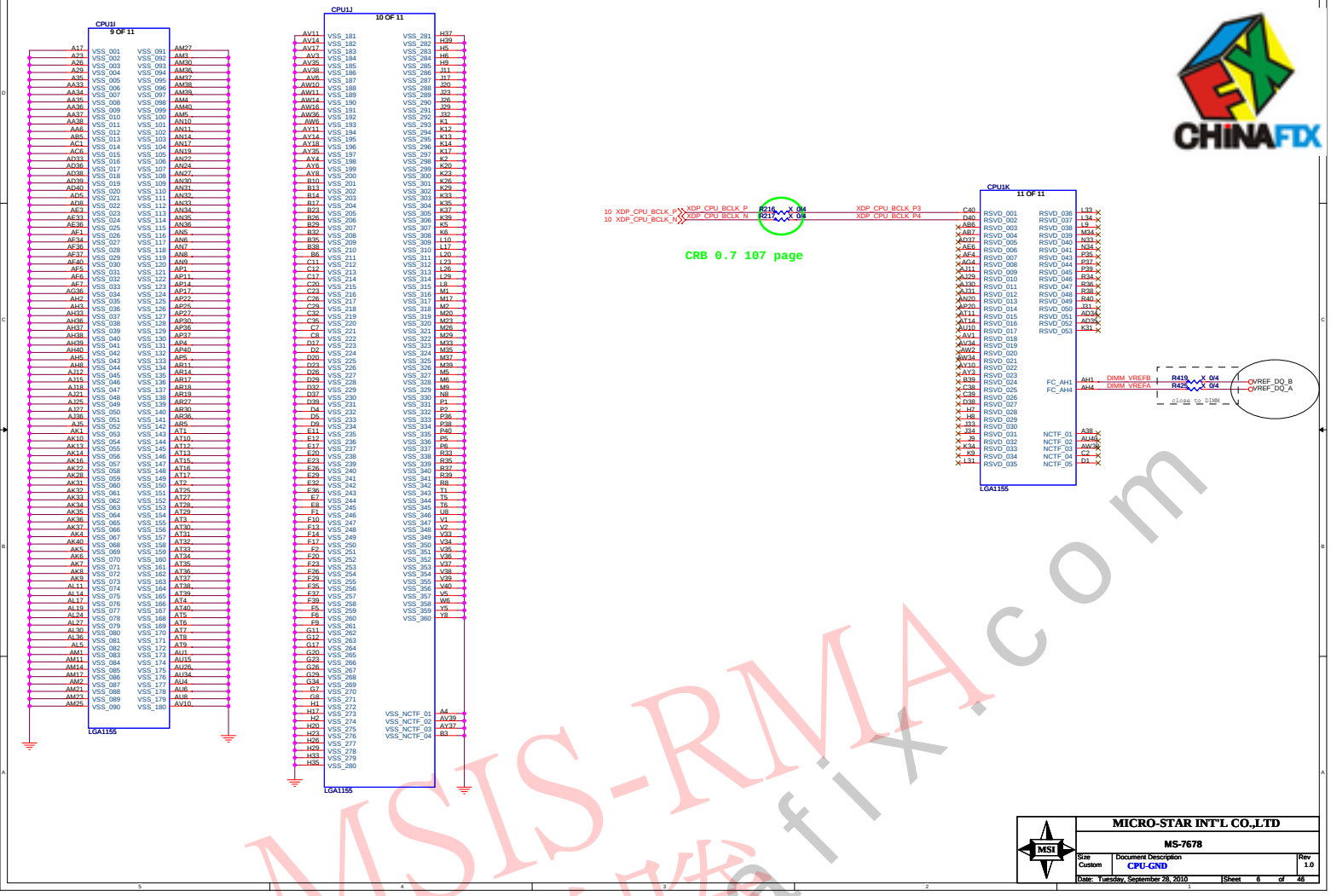

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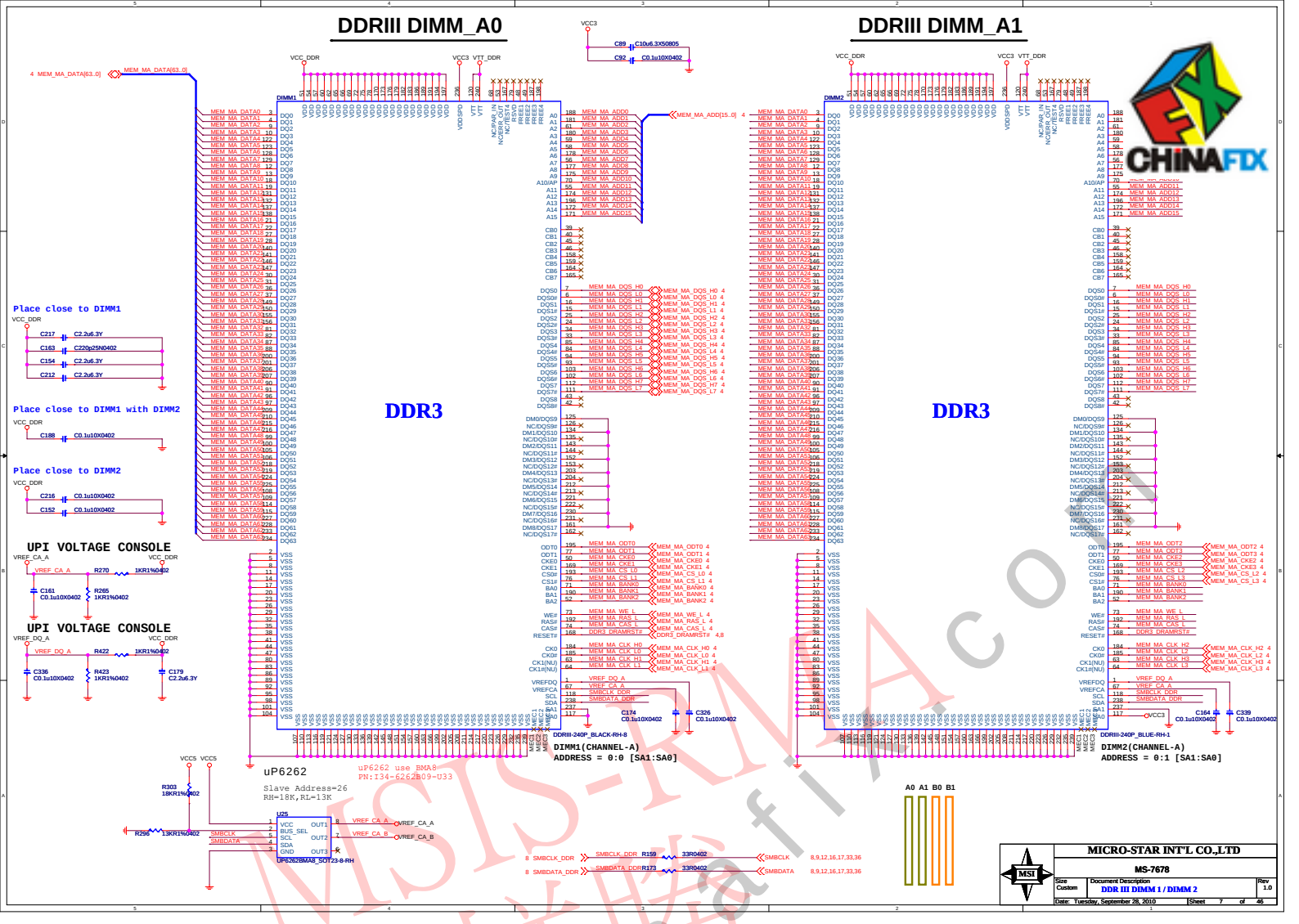

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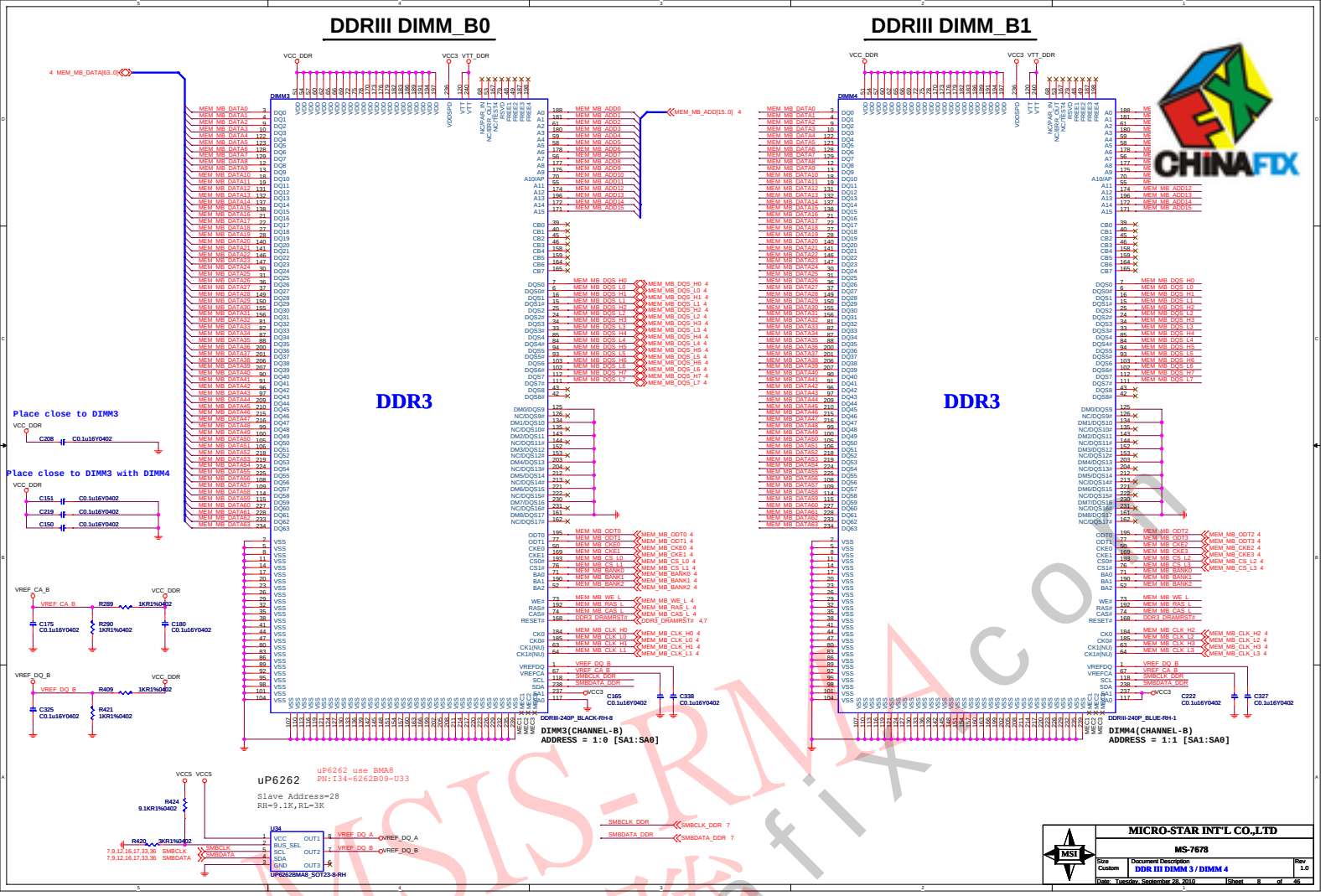

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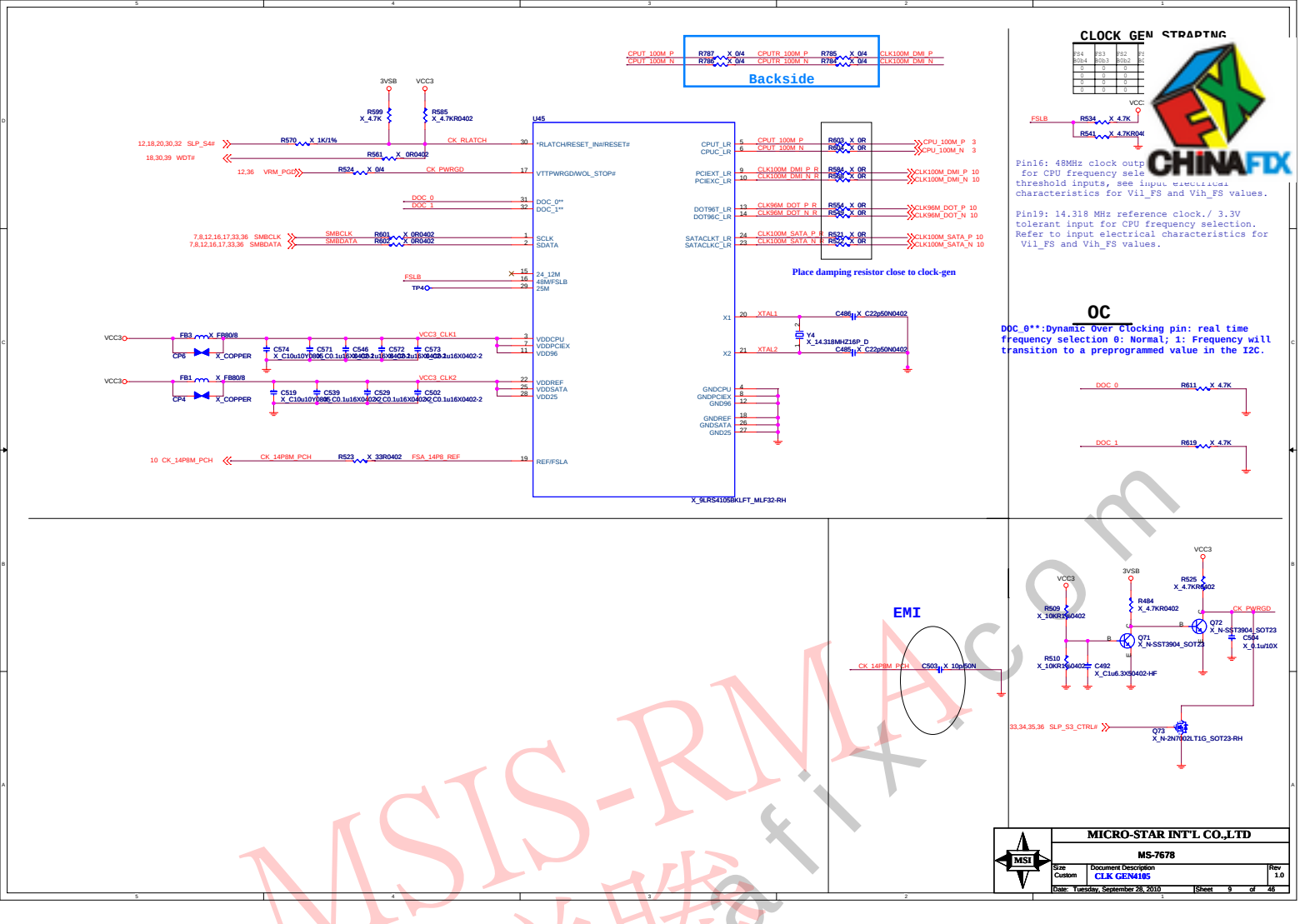

CLOCK GEN STRAPPING

FS4	FS3	FS2	FS
SB0b4	SB0b3	SB0b2	SB
0	0	0	
0	0	0	
0	0	0	
0	0	0	

Pin16: 48MHz clock outp
for CPU frequency sele
threshold inputs, see Input Electrical
characteristics for Vil_FS and Vih_FS values.

Pin19: 14.318 MHz reference clock./ 3.3V
tolerant input for CPU frequency selection.
Refer to input electrical characteristics for
Vil_FS and Vih_FS values.

OC

DOC_0**:Dynamic Over Clocking pin: real time frequency selection 0: Normal; 1: Frequency will transition to a preprogrammed value in the I2C.

EMI

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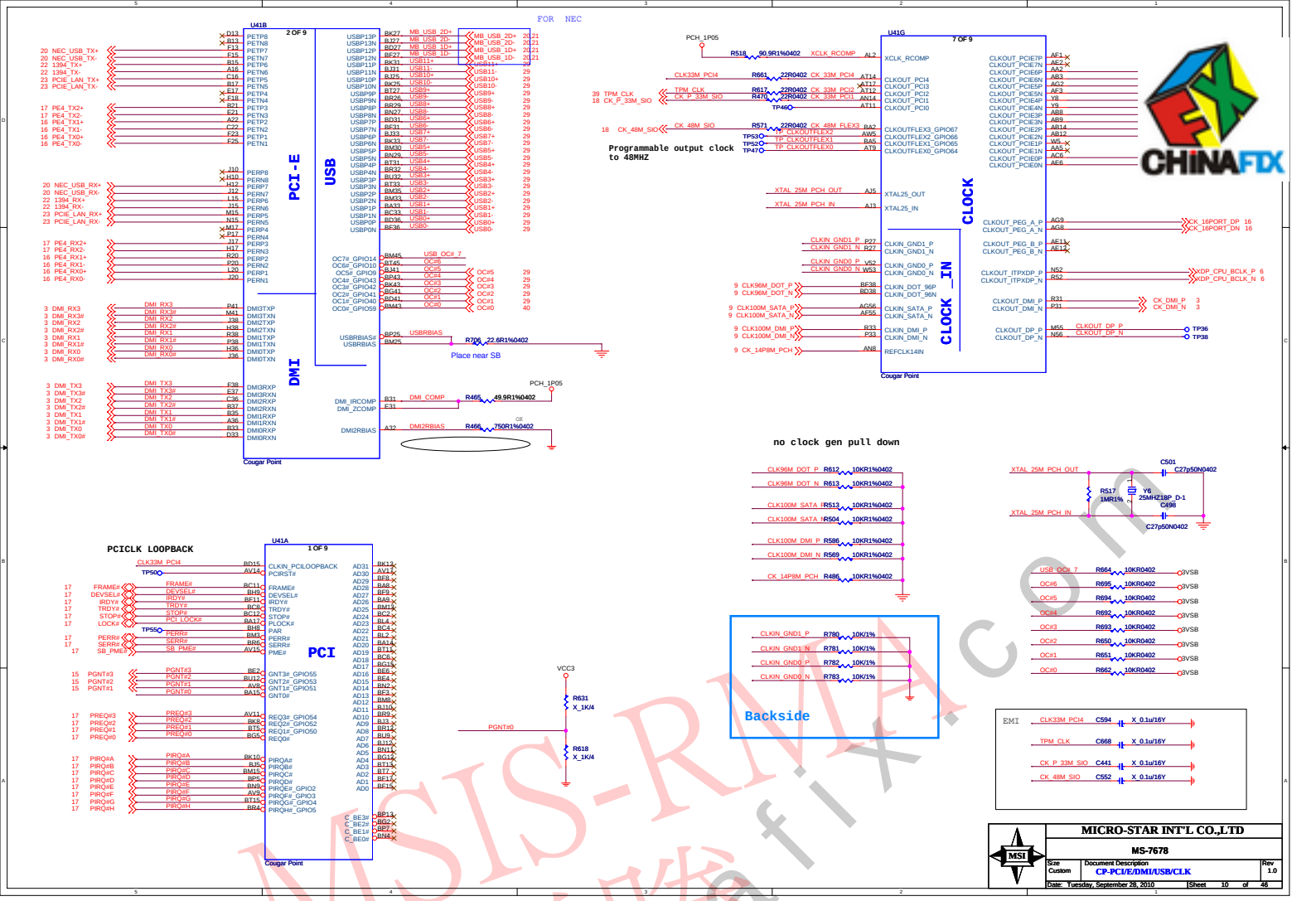

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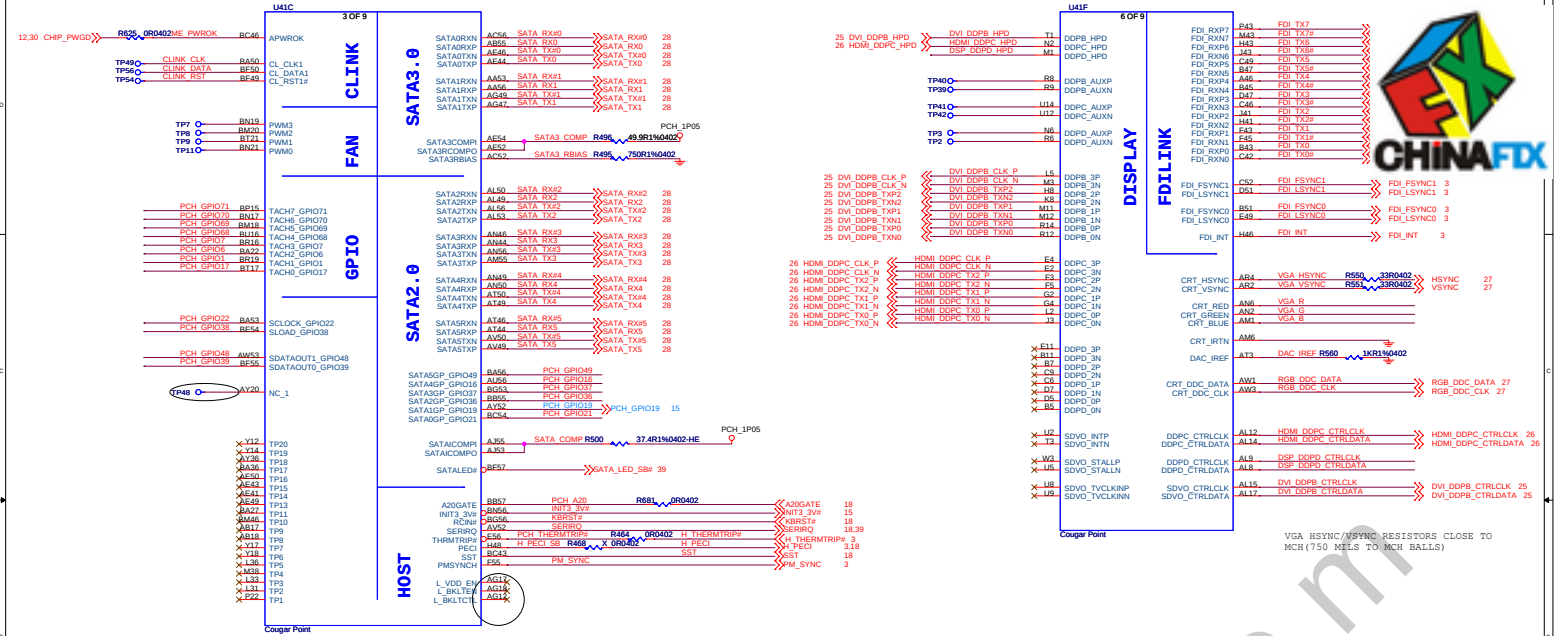
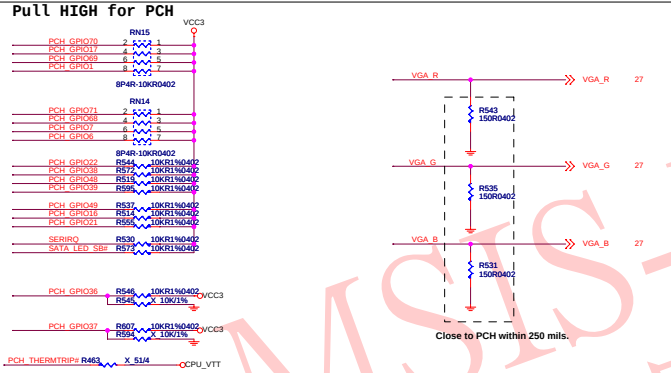
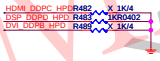


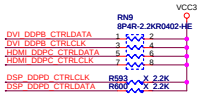
Pull HIGH for PCH



No VGA(pull down)



Enable VGA(CTRLCLK/DATA Pull High)



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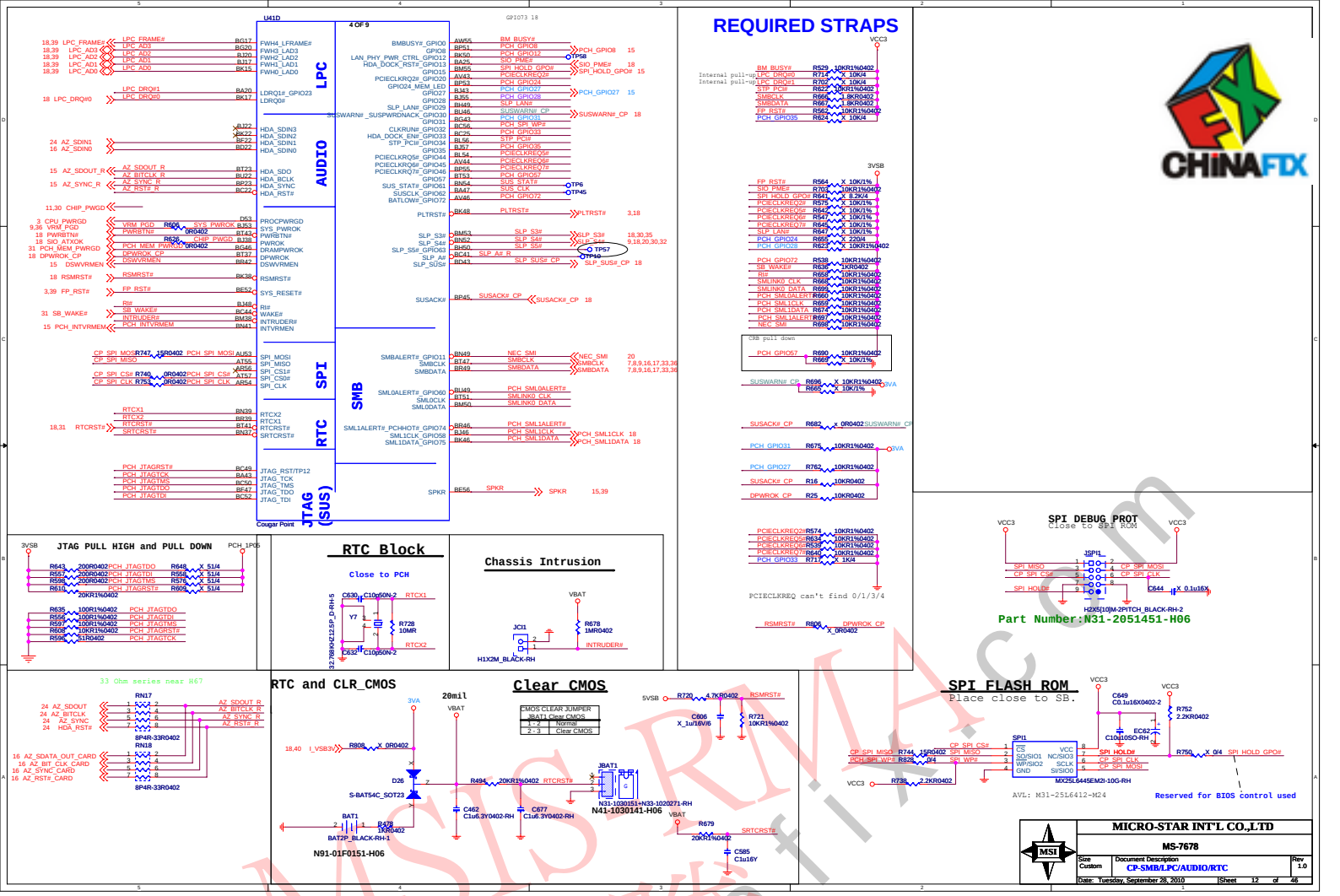

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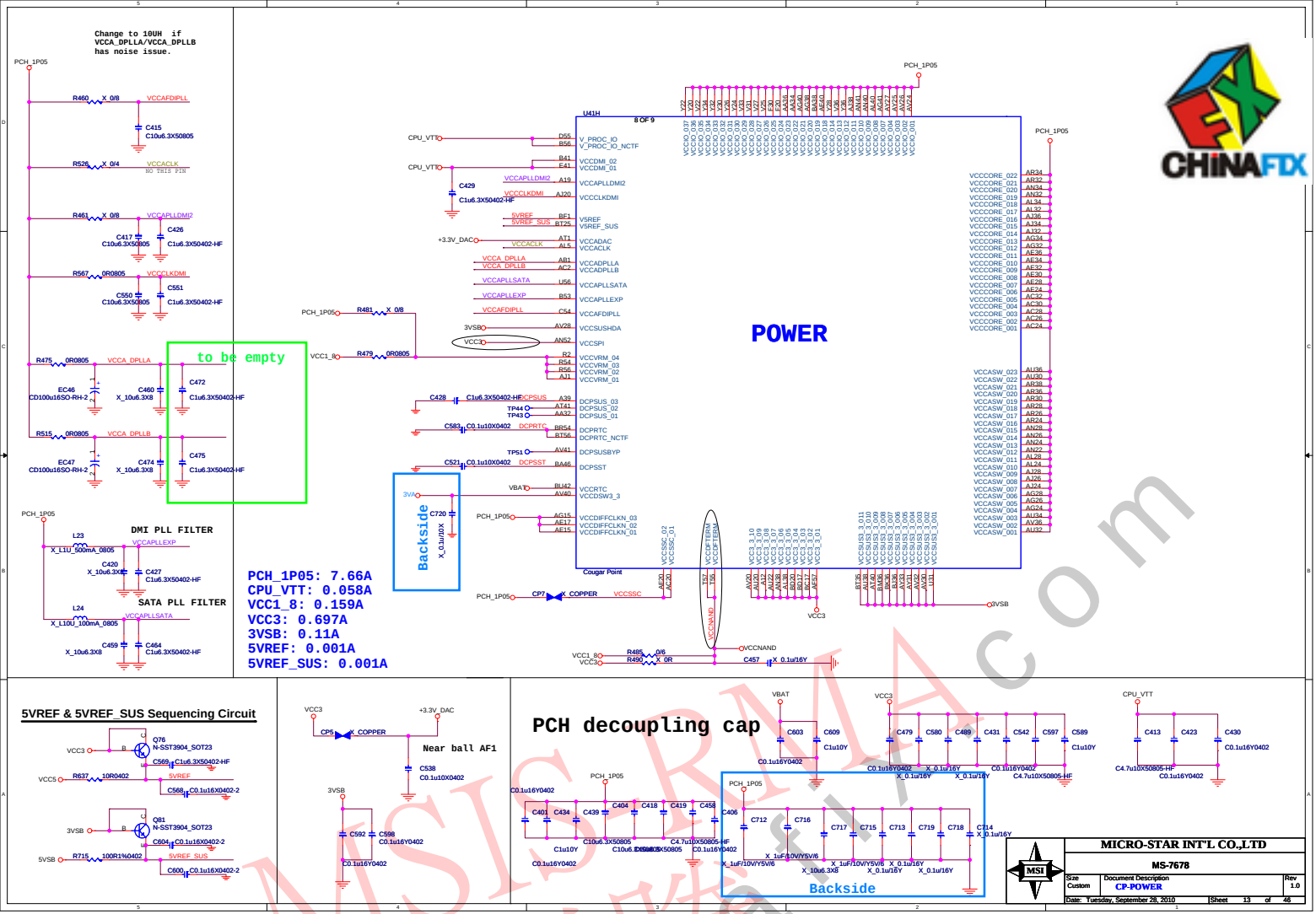

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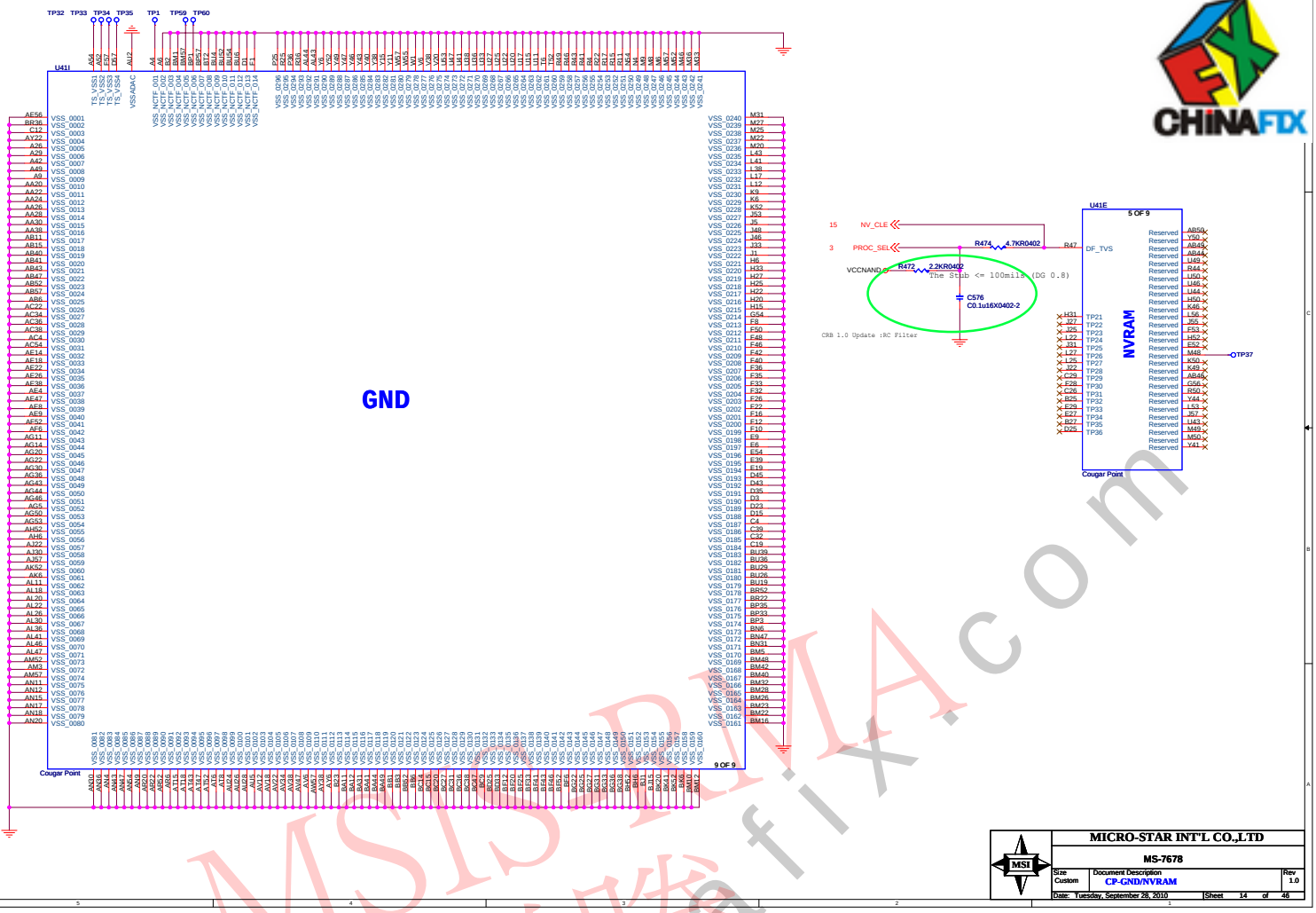

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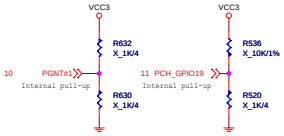
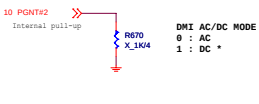
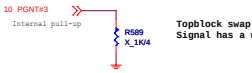
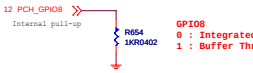
PCH Straps

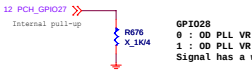
BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1



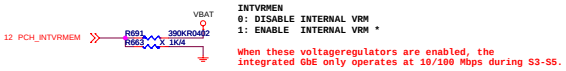


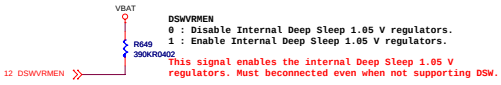


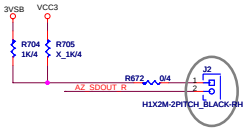


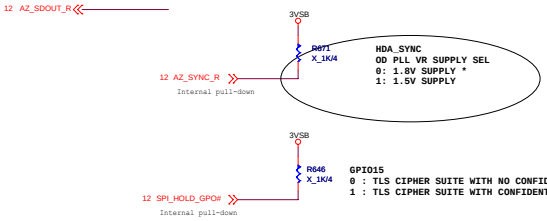


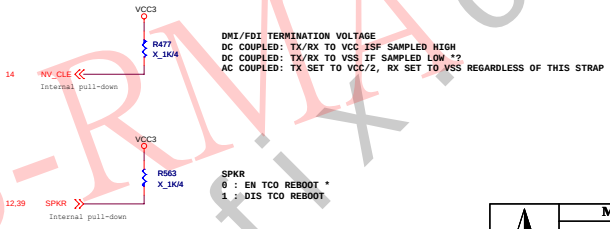
1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.











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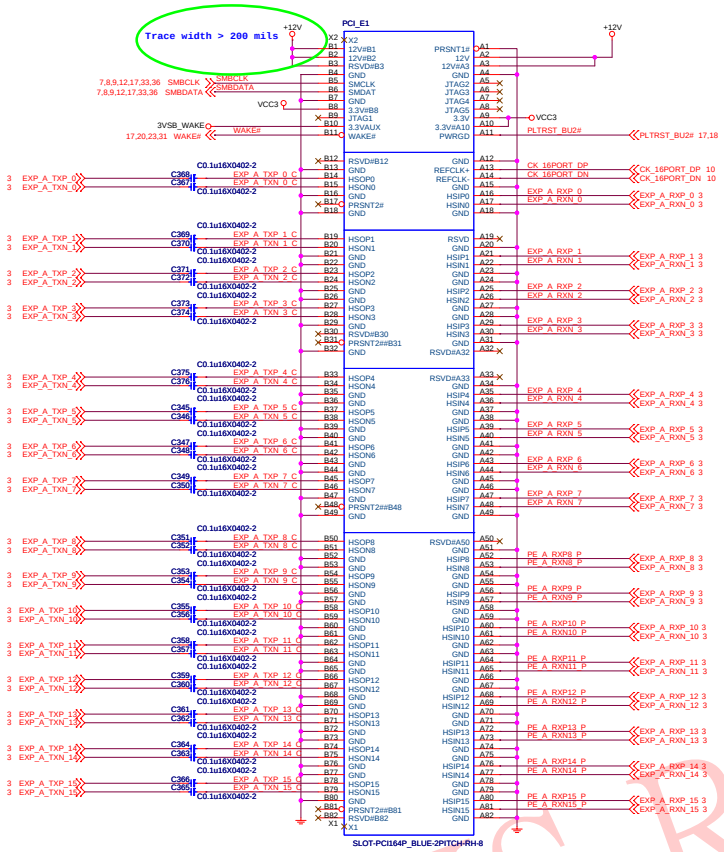
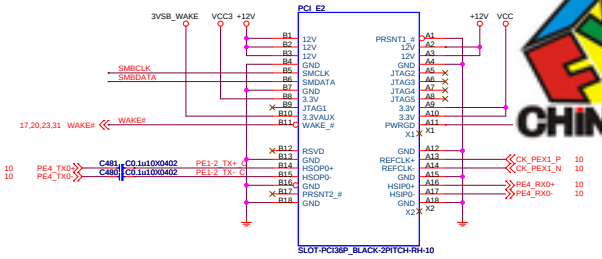
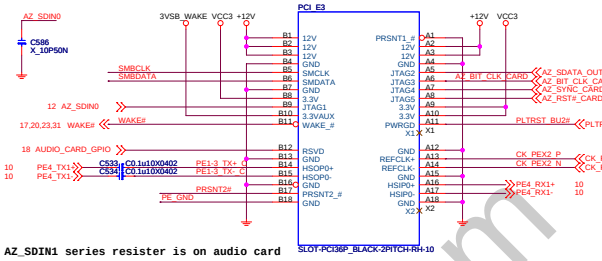
PCI_Express X16 Slot



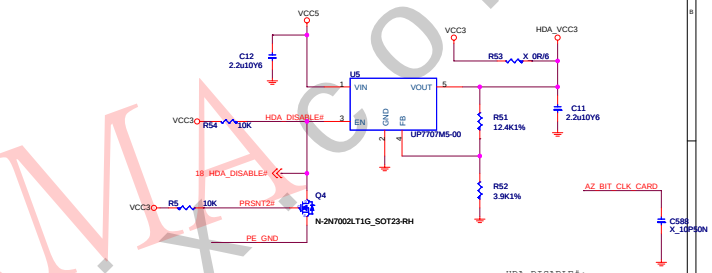
PCI EXPRESS x1-PORT



PCI EXPRESS x1-PORT

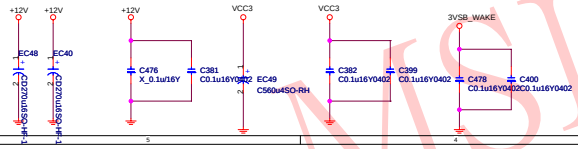


AZ_SDIN1 series resister is on audio card



HDA_DISABLE#:
to SIO GPI047 ,pin14
Hi: onboard codec Verb table
Low: PCIE Audio Verb table

	PE1X1_PRSNT#	PE_GND
Other board	0	0
4132 audio	1	0
N/A	1	N/C



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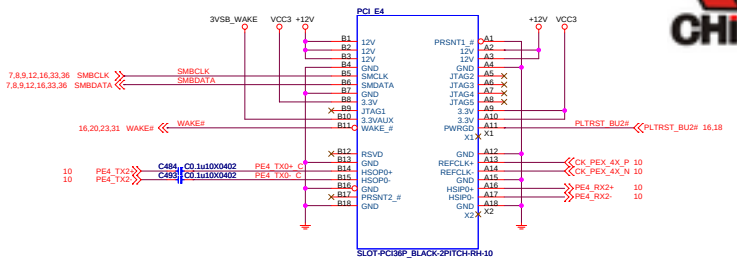
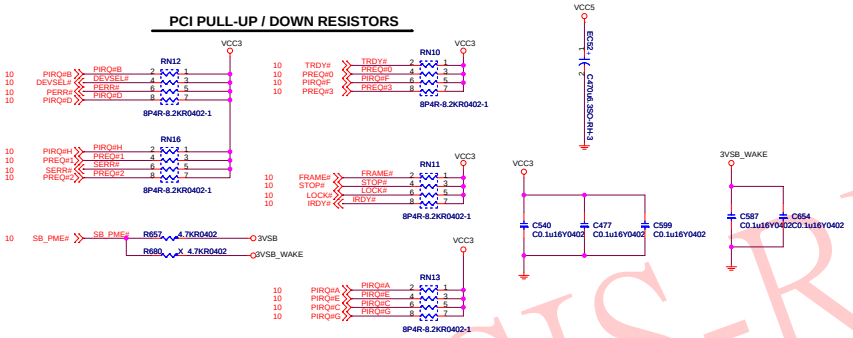
PCI EXPRESS x1-PORT



PCI PULL-UP / DOWN RESISTORS



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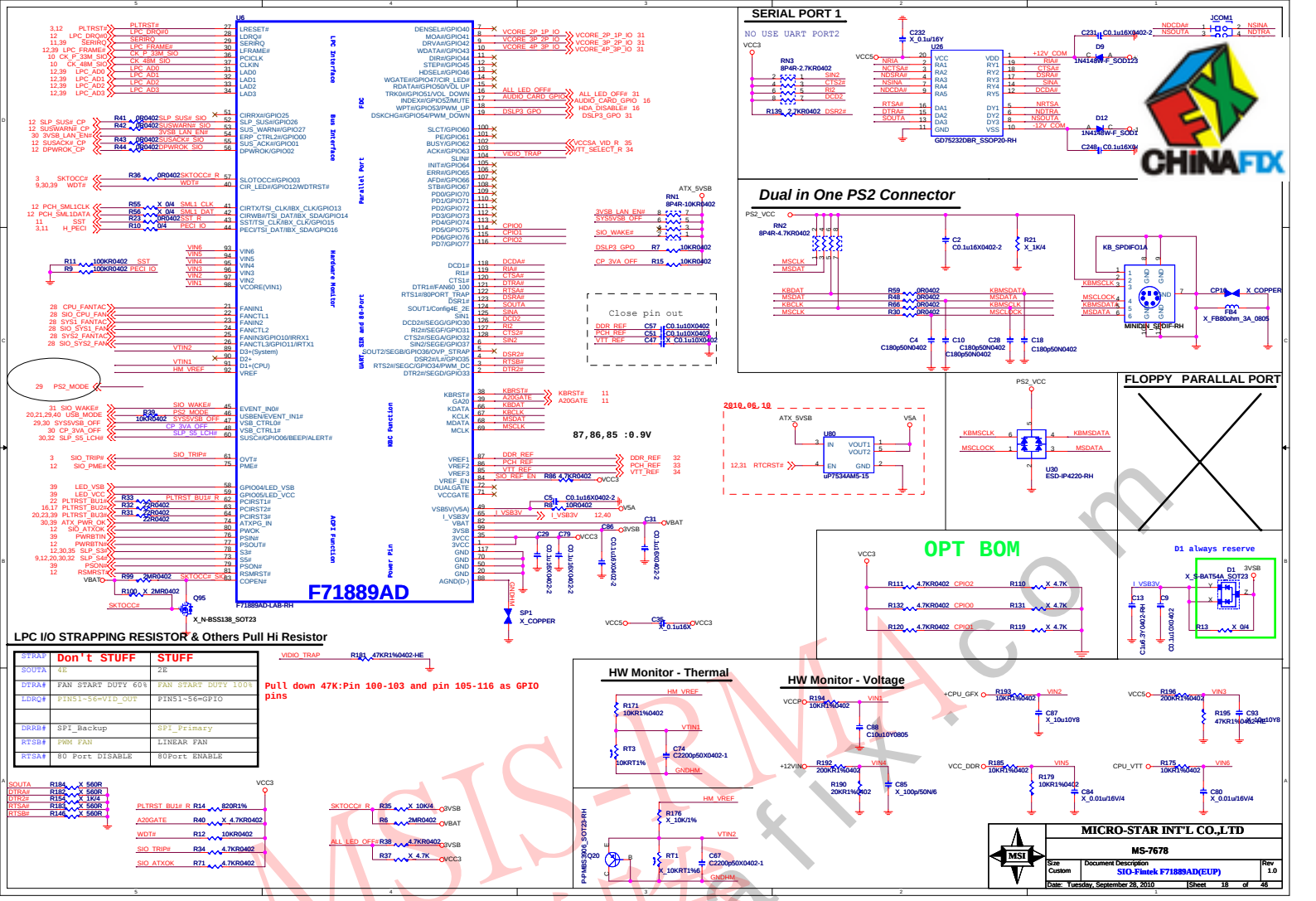

STRAP	Don't STUFF	STUFF
SOUTA	4E	2E
DTRA#	FAN START DUTY 60%	FAN START DUTY 100%
LDRQ#	PIN51~56=VID_OUT	PIN51~56=GPIO
DRRB#	SPI_Backup	SPI_Primary
RTSB#	PWM FAN	LINEAR FAN
RTSA#	80 Port DISABLE	80Port ENABLE

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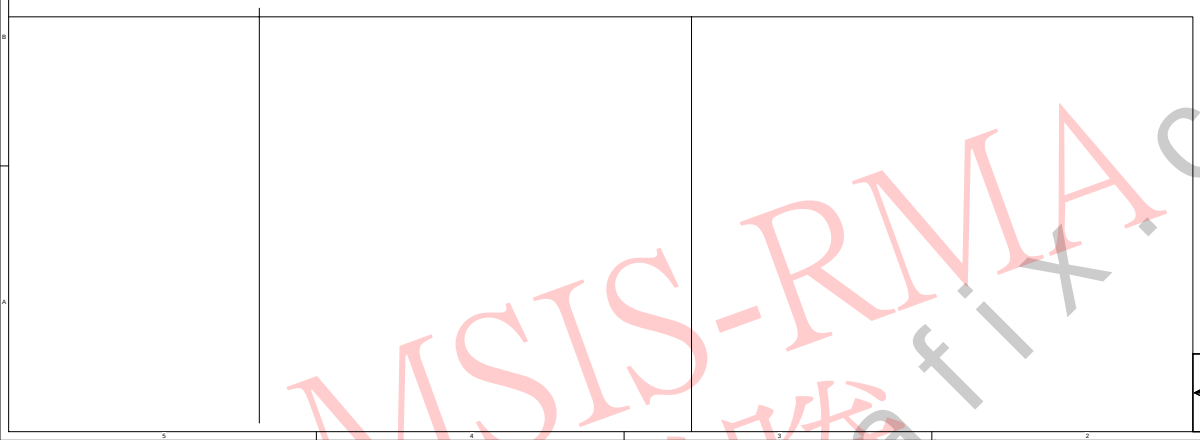

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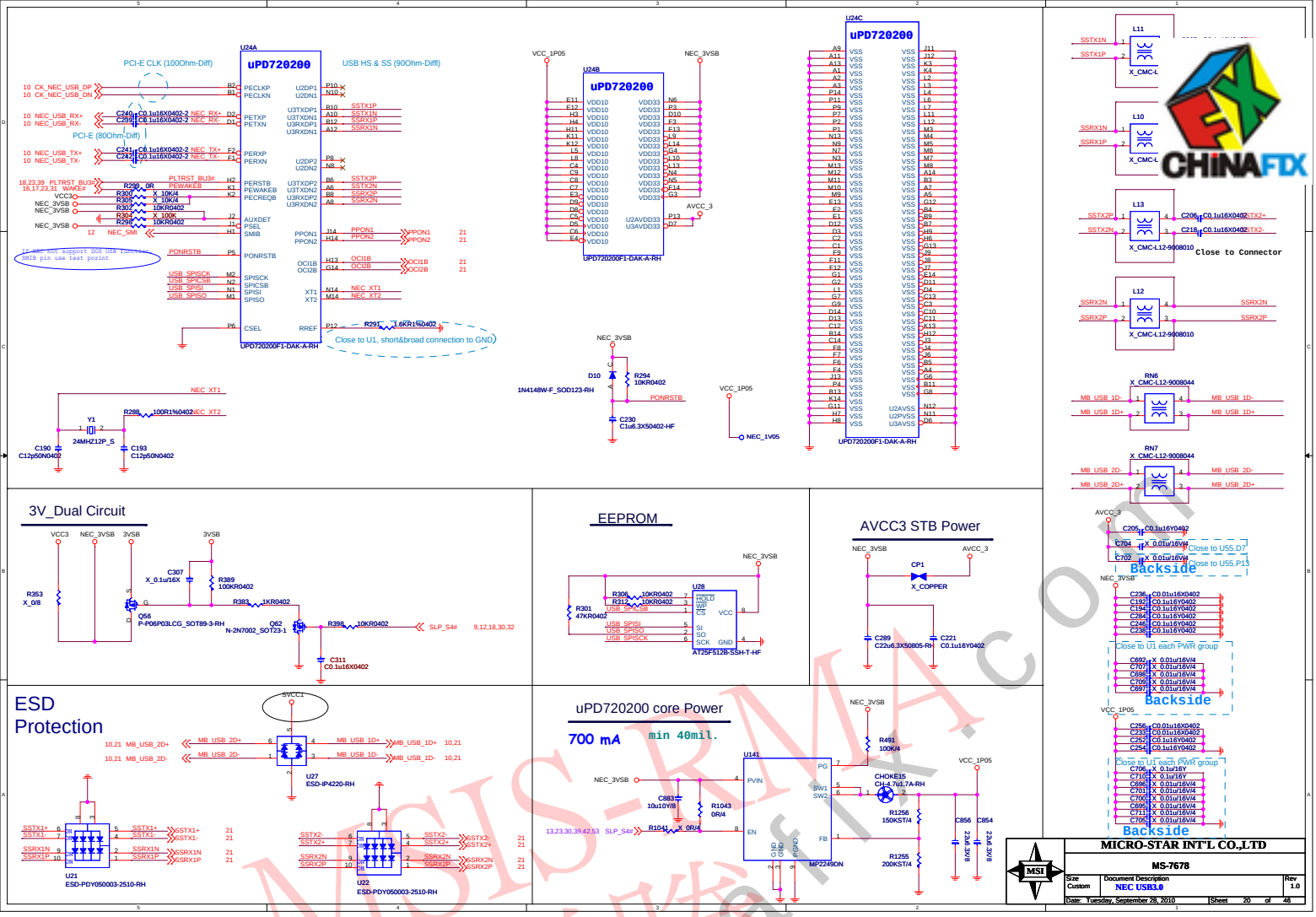

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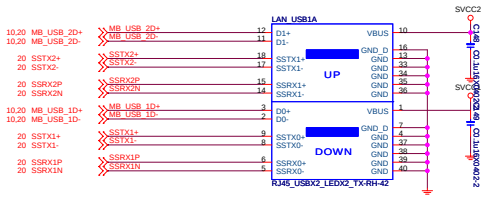
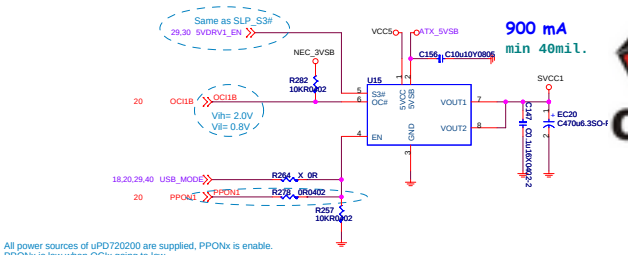
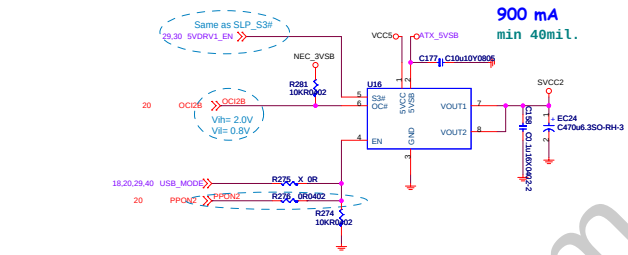




All power sources of uPD720200 are supplied, PPONx is enable.
PPONx is low when OCIx going to low.



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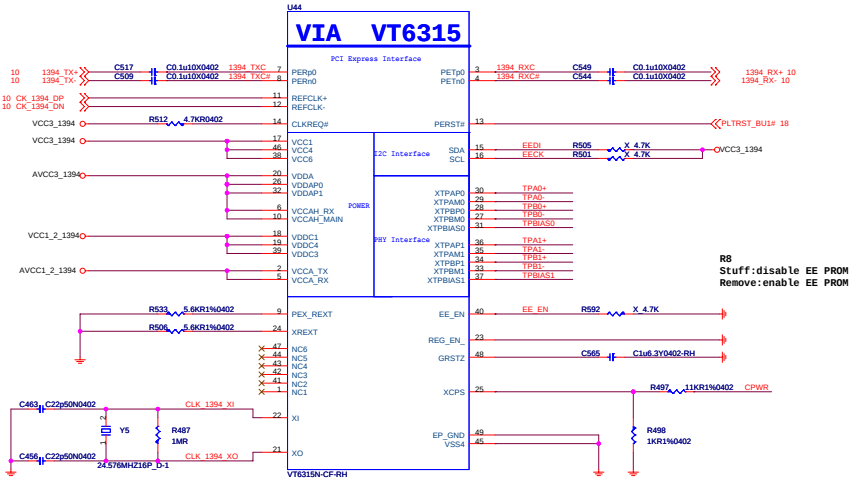
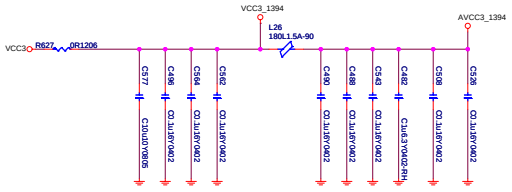
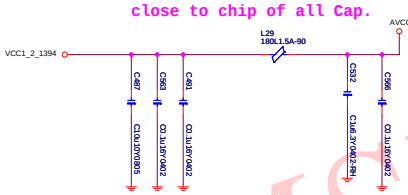
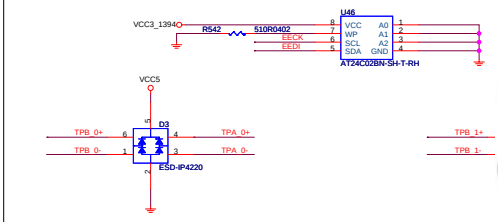
1394 CONTROLLER



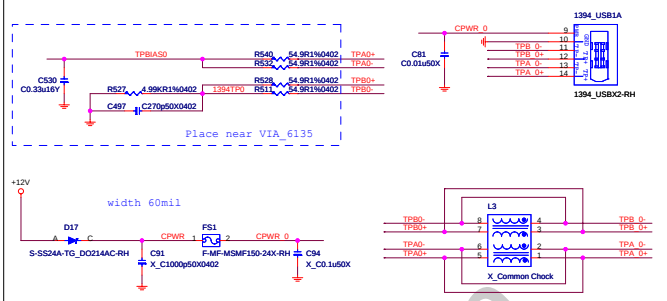




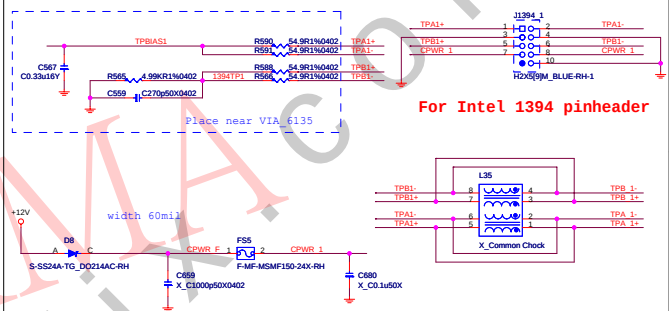
EE PROM



Rear 1394 port



Front 1394 pin header



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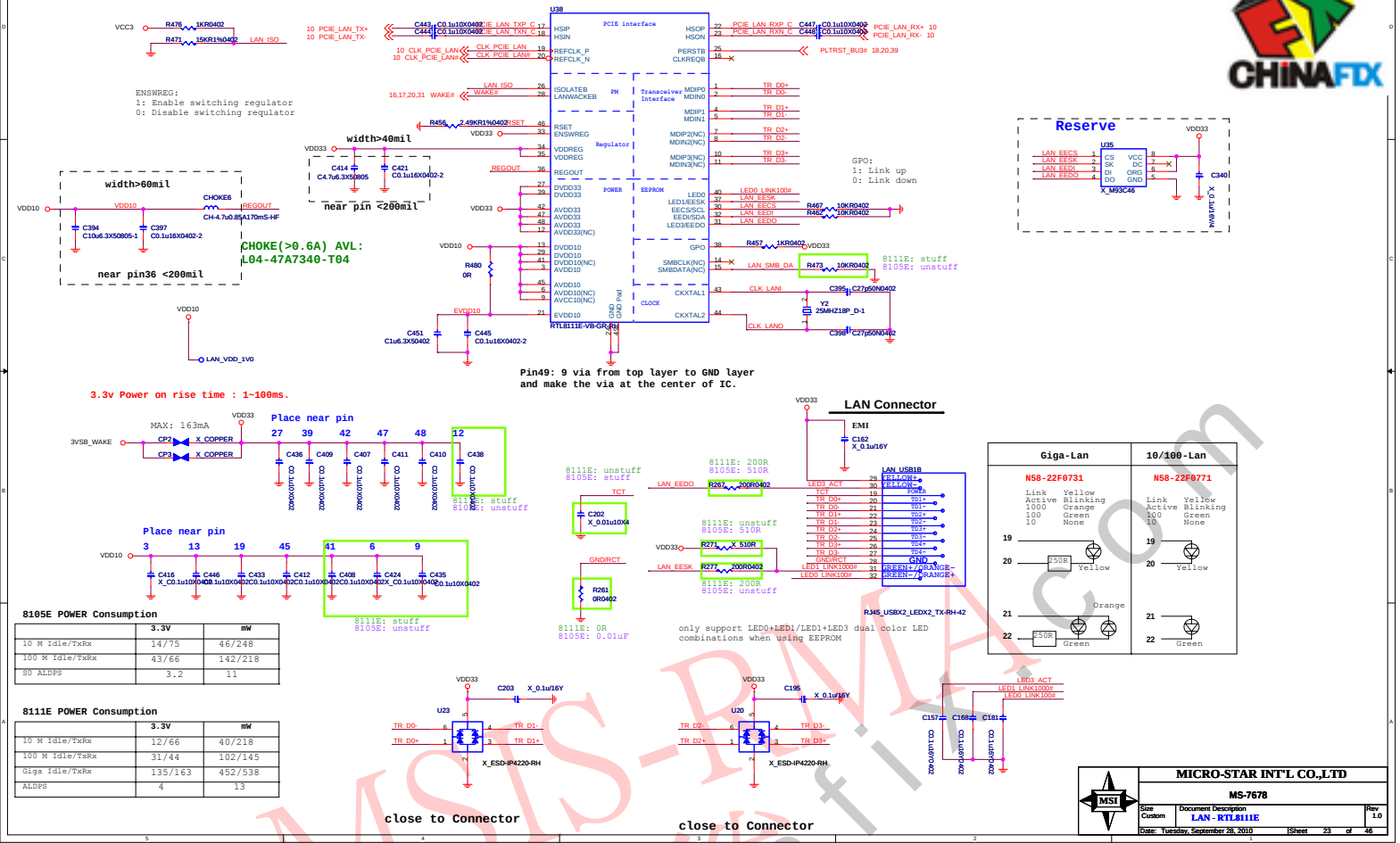
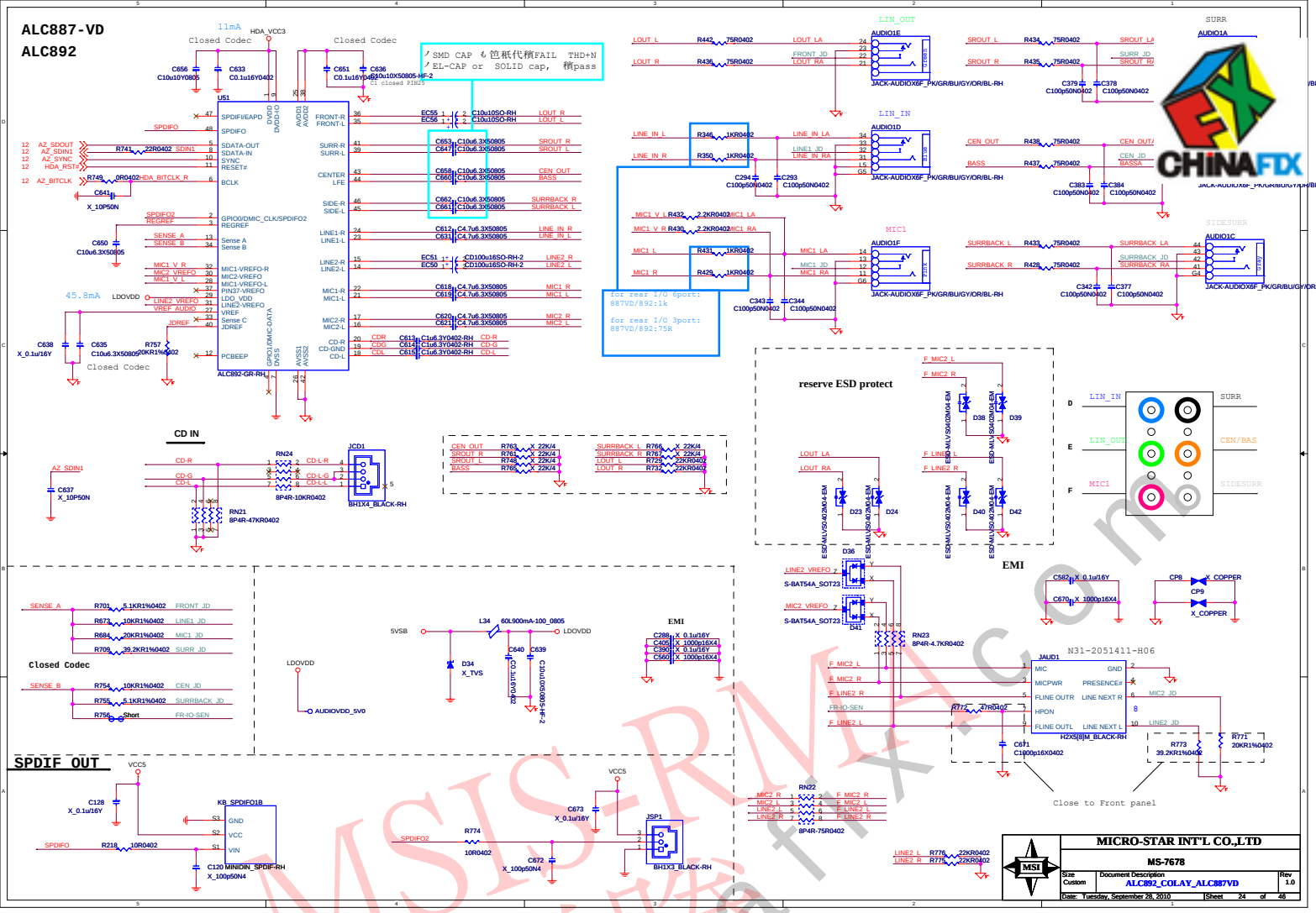
RTL8111E Giga LAN

RTL8105E 10/100M LAN





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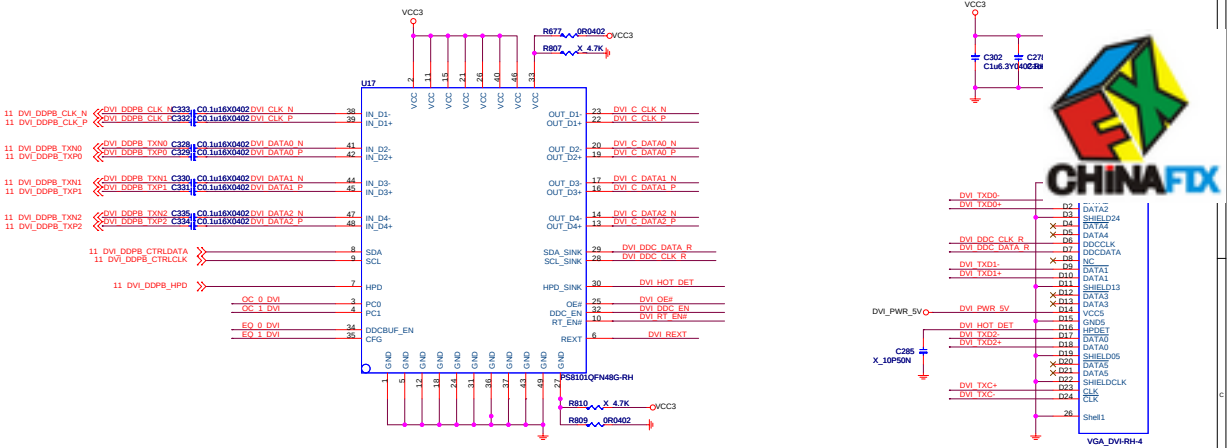
DVI level shifter



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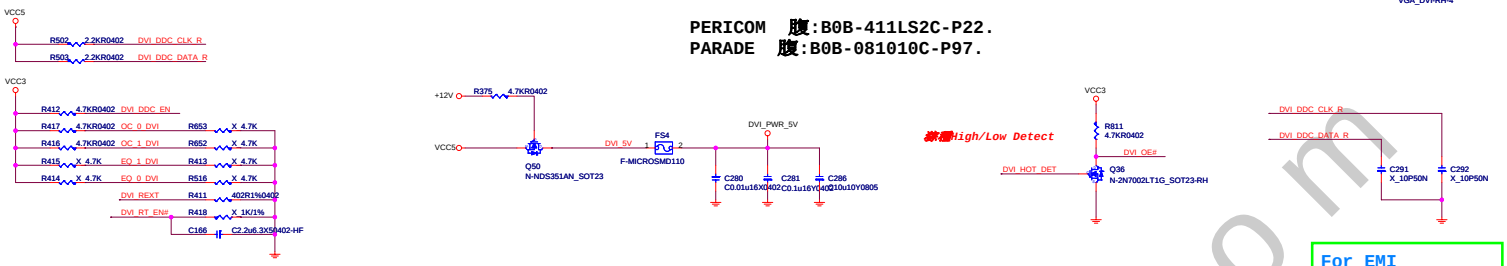
PARADE 腹:B0B-081010C-P97.

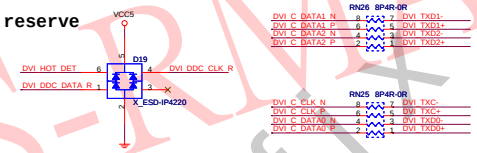


	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifitng configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

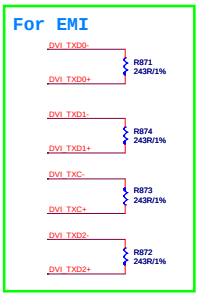
[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

reserve



For EMI



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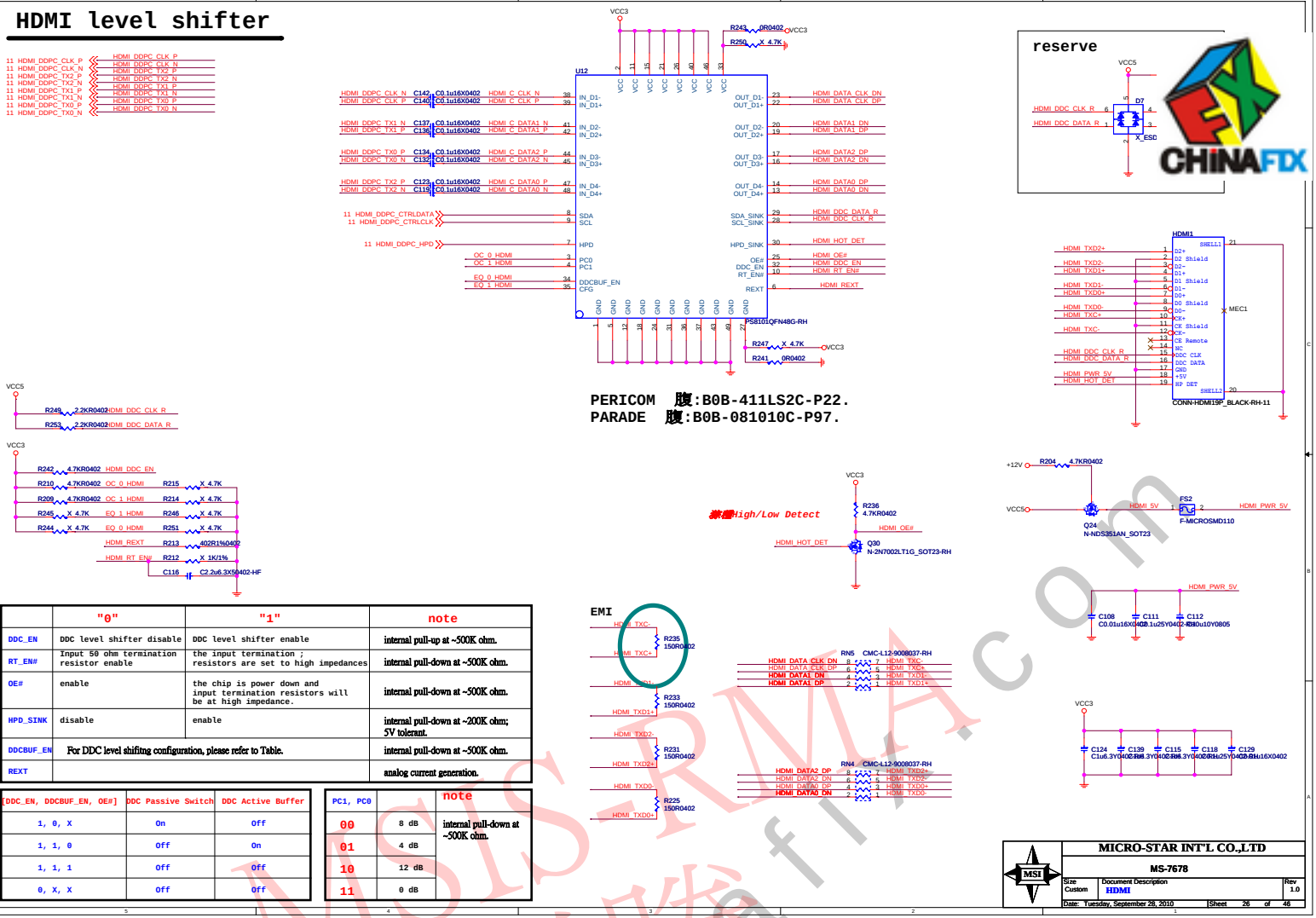
HDMI level shifter



	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifitng configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

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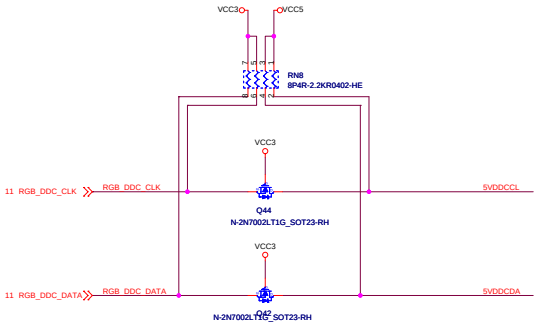
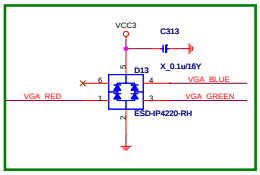
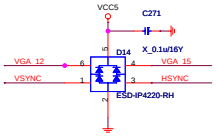
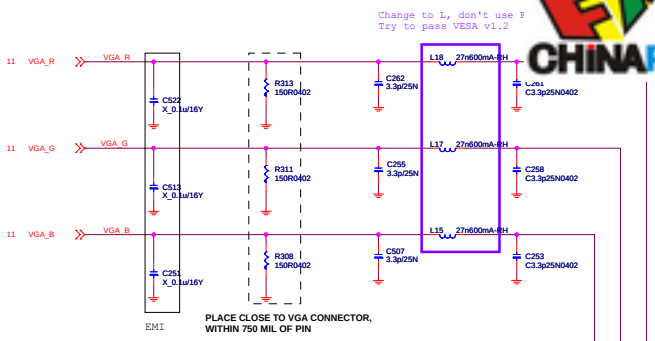
D-Sub

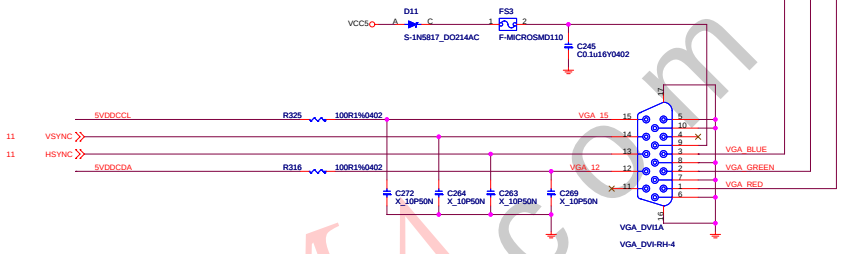
Level shift











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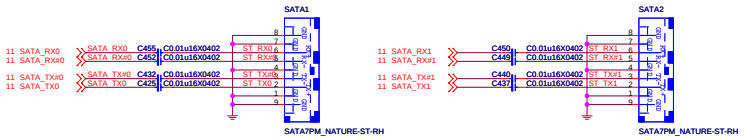
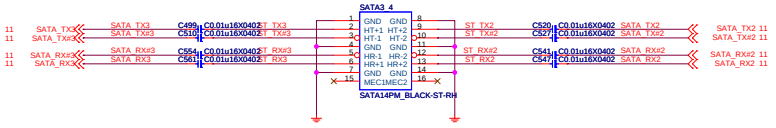
SATA 6G PORT 0,1

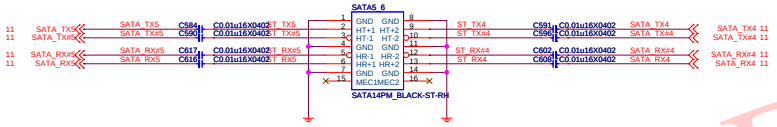


For B65,SATA2 should change to Gen2

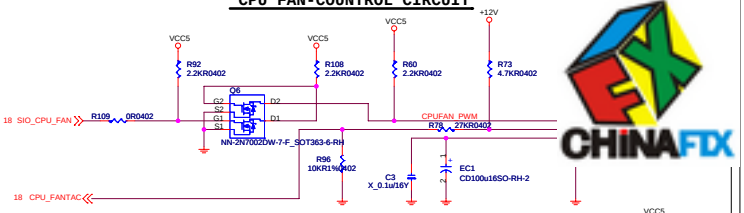
SATA 3G PORT 2,3



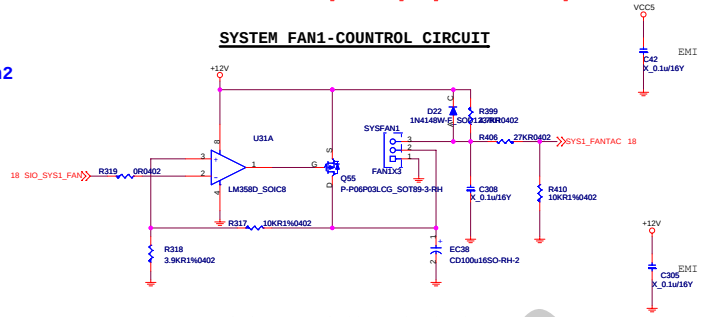
SATA 3G PORT 4,5



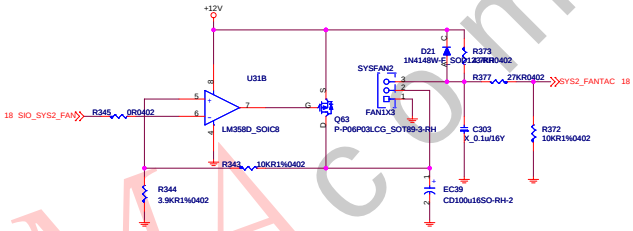
CPU FAN-COUNTROL CIRCUIT



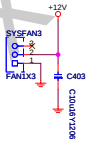
SYSTEM FAN1-COUNTROL CIRCUIT



SYSTEM FAN2-COUNTROL CIRCUIT



SYSTEM FAN3-12V



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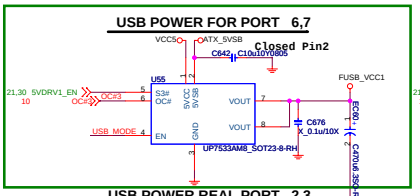
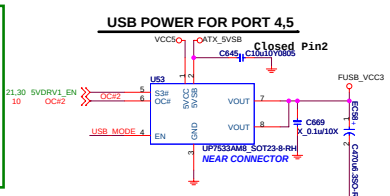
Front USB Connector

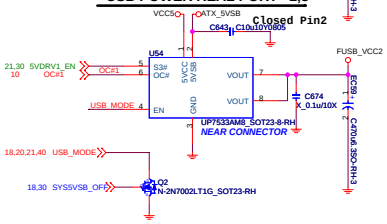
USB POWER FOR PORT 6,7



USB POWER FOR PORT 4,5

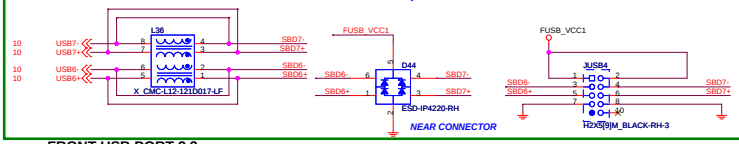


USB POWER REAL PORT 2,3

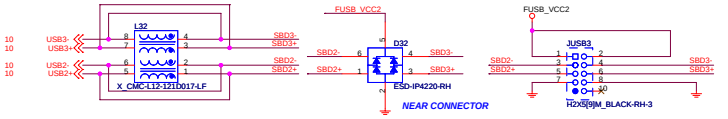


FRONT USB PORT 0,1

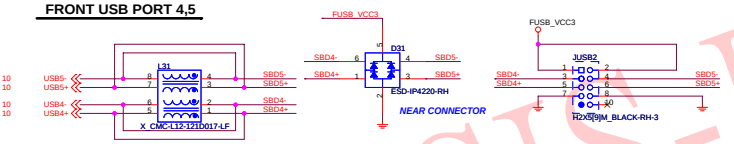
For B65,JUSB4 should be remove



FRONT USB PORT 2,3

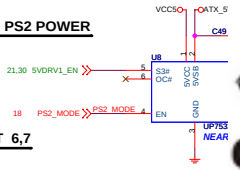


FRONT USB PORT 4,5

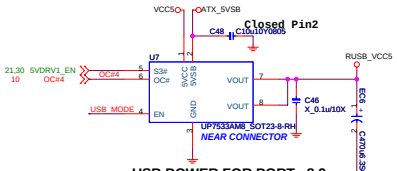


Rear USB Connector

PS2 POWER

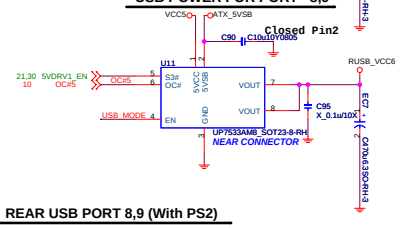


USB POWER FOR PORT 6,7

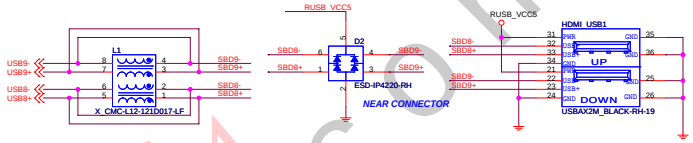


USB_MODE for USB voltage
H:Follow 5VSB
L:Always off

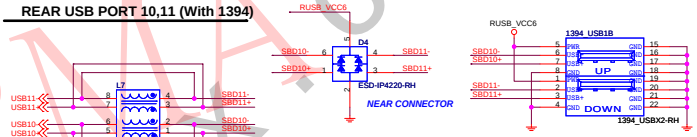
USB POWER FOR PORT 8,9



REAR USB PORT 8,9 (With PS2)



REAR USB PORT 10,11 (With 1394)



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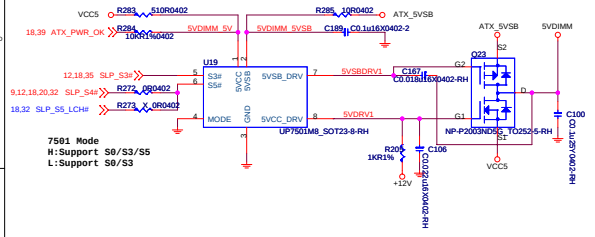
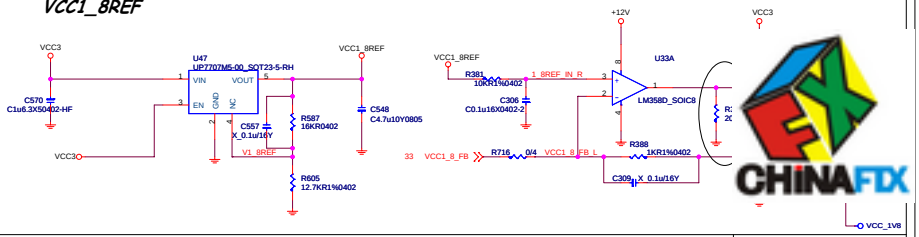
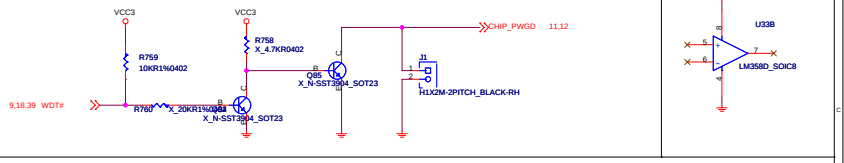
5VDIMM FOR DDR



VCC1_8REF

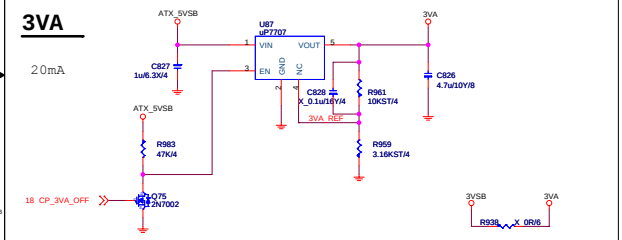


WATCH DOG

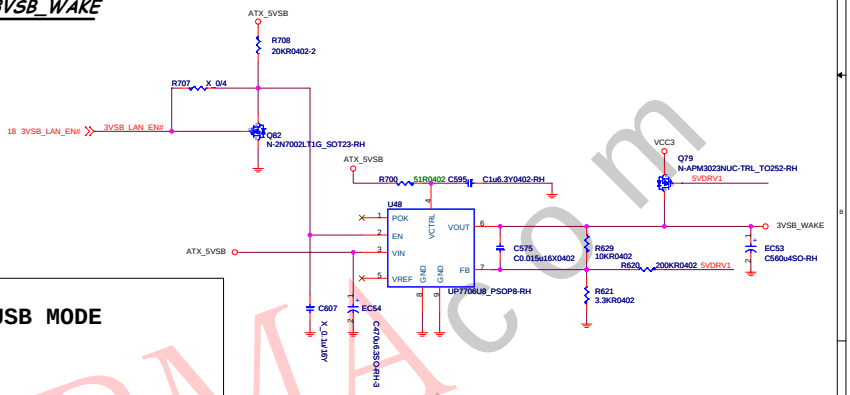


3VA

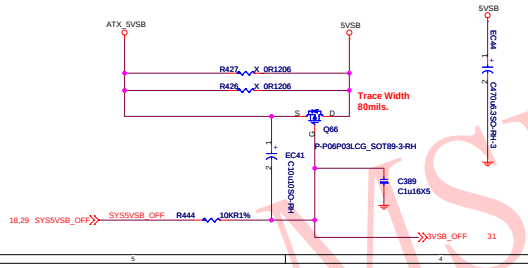
20mA



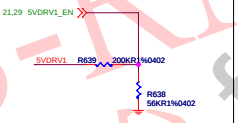
3VSB_WAKE



5VSB Power Switch



USB MODE



3VSB supply to PCH and other device. Turn off when Deep S3/S5.
+3VSB_WAKE supply to PCI Slot and LAN power.Turn off when Deep S3/S5 w/o WOL.

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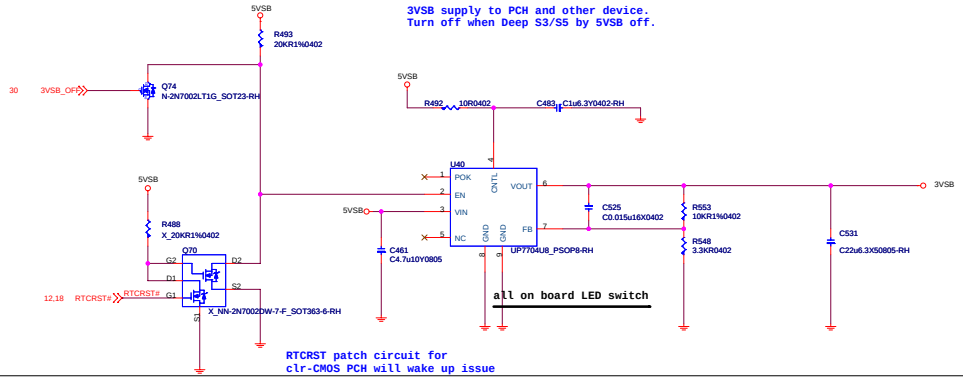
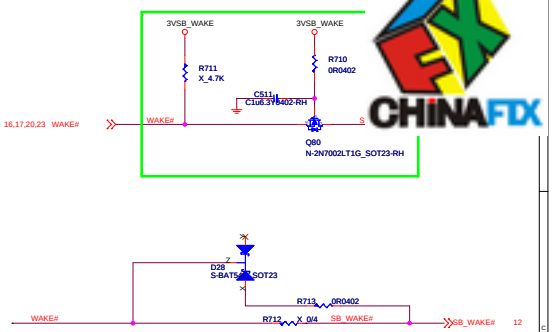
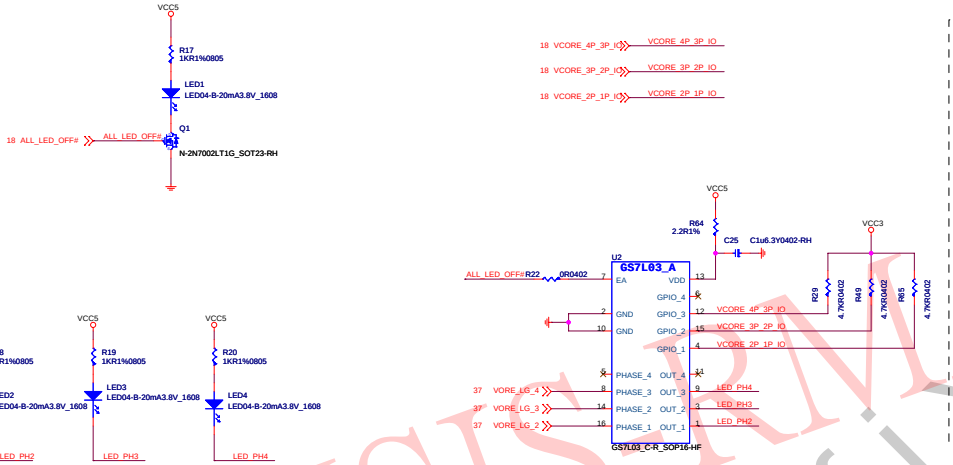
Deep Mode WOL LAN Power CTRL Circuit

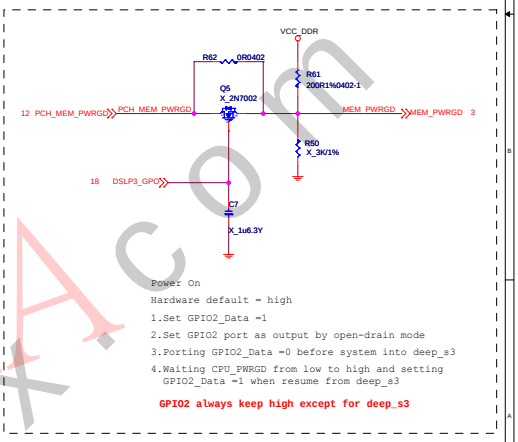


LAN/PCIE/PCI Wake Up CTRL Circuit



APS & LED





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DDR3_1.5V 4.5A+15A+1A=20.5A

4.5A FOR CPU

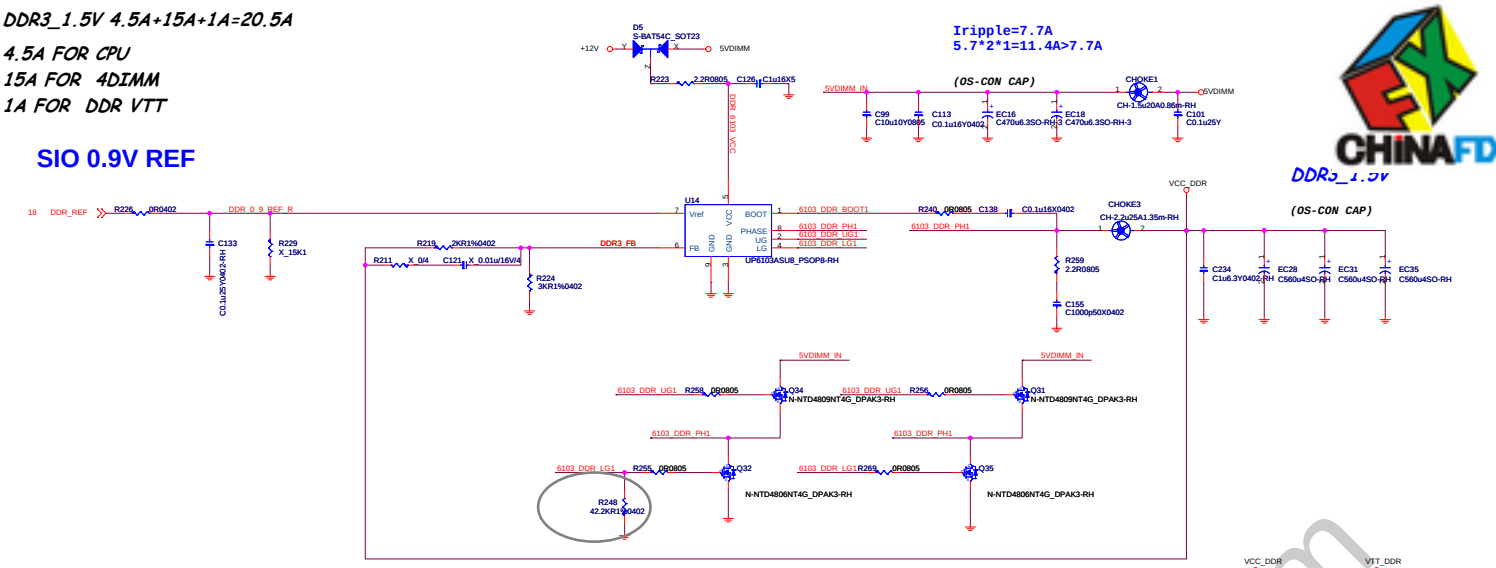
15A FOR 4DIMM

1A FOR DDR VTT

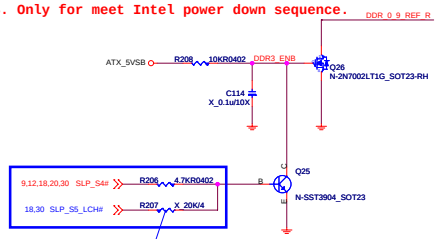
SIO 0.9V REF

Iripple=7.7A

5.7*2*1=11.4A>7.7A



P.S. Only for meet Intel power down sequence.

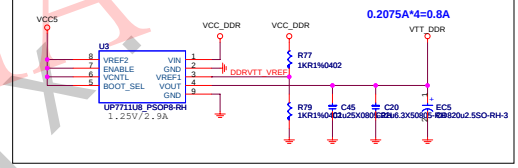


For Deep_S3 Mode

DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

0.2075A*4=0.8A



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Size: Custom	Document Description: DDR Power - uP6103 1-Phase	Rev: 1.0
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PCH Power:1.05V

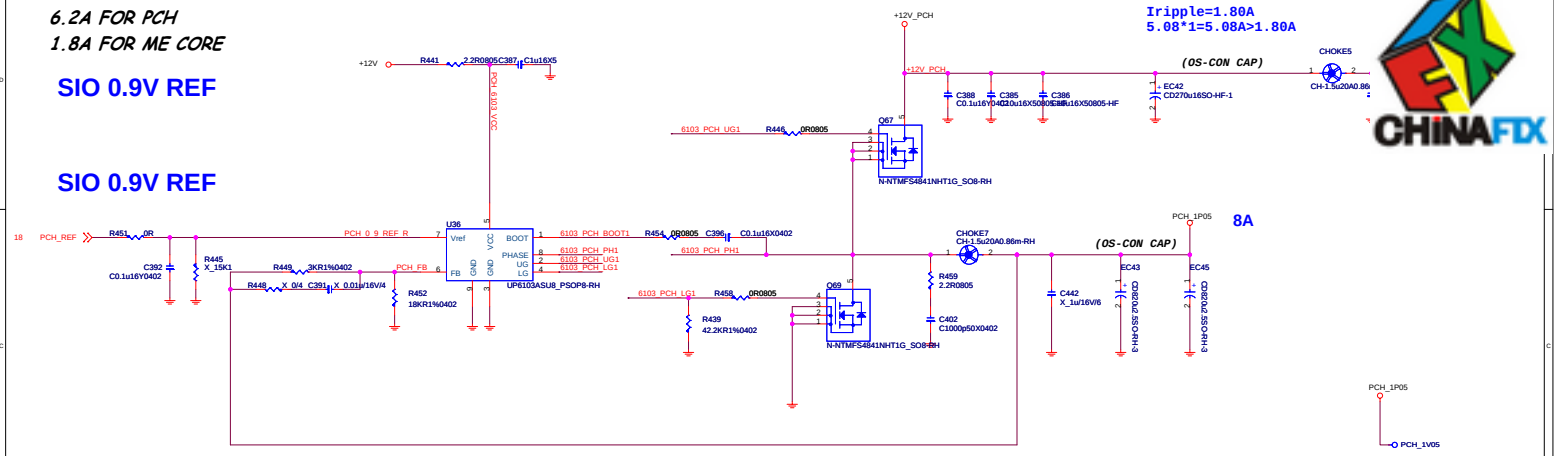
PCH Core 6.2A+1.8A=8A

6.2A FOR PCH

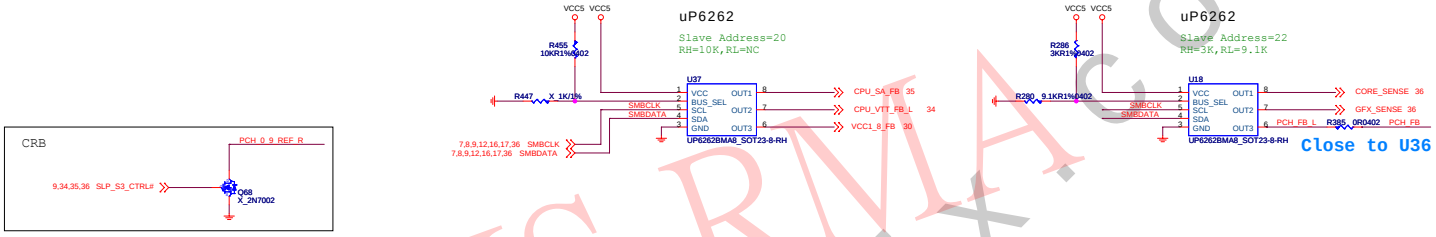
1.8A FOR ME CORE

SIO 0.9V REF

SIO 0.9V REF



UPI VOLTAGE CONSOLE



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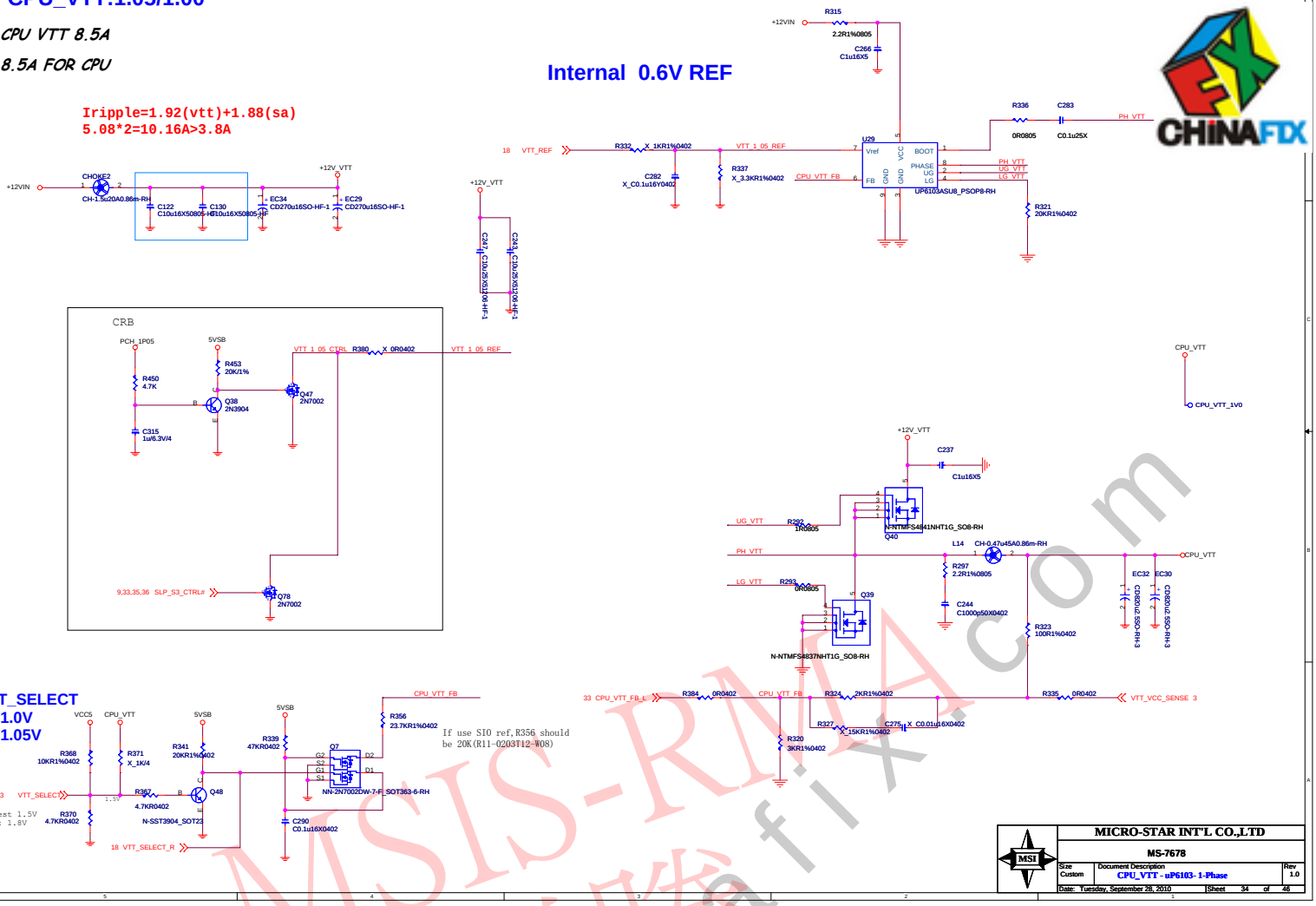
CPU_VTT:1.05/1.00

CPU VTT 8.5A

8.5A FOR CPU

Iripple=1.92(vtt)+1.88(sa)
5.08*2=10.16A>3.8A

Internal 0.6V REF



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Size: Custom	Document Description: CPU_VTT - uP6103-1-Phase
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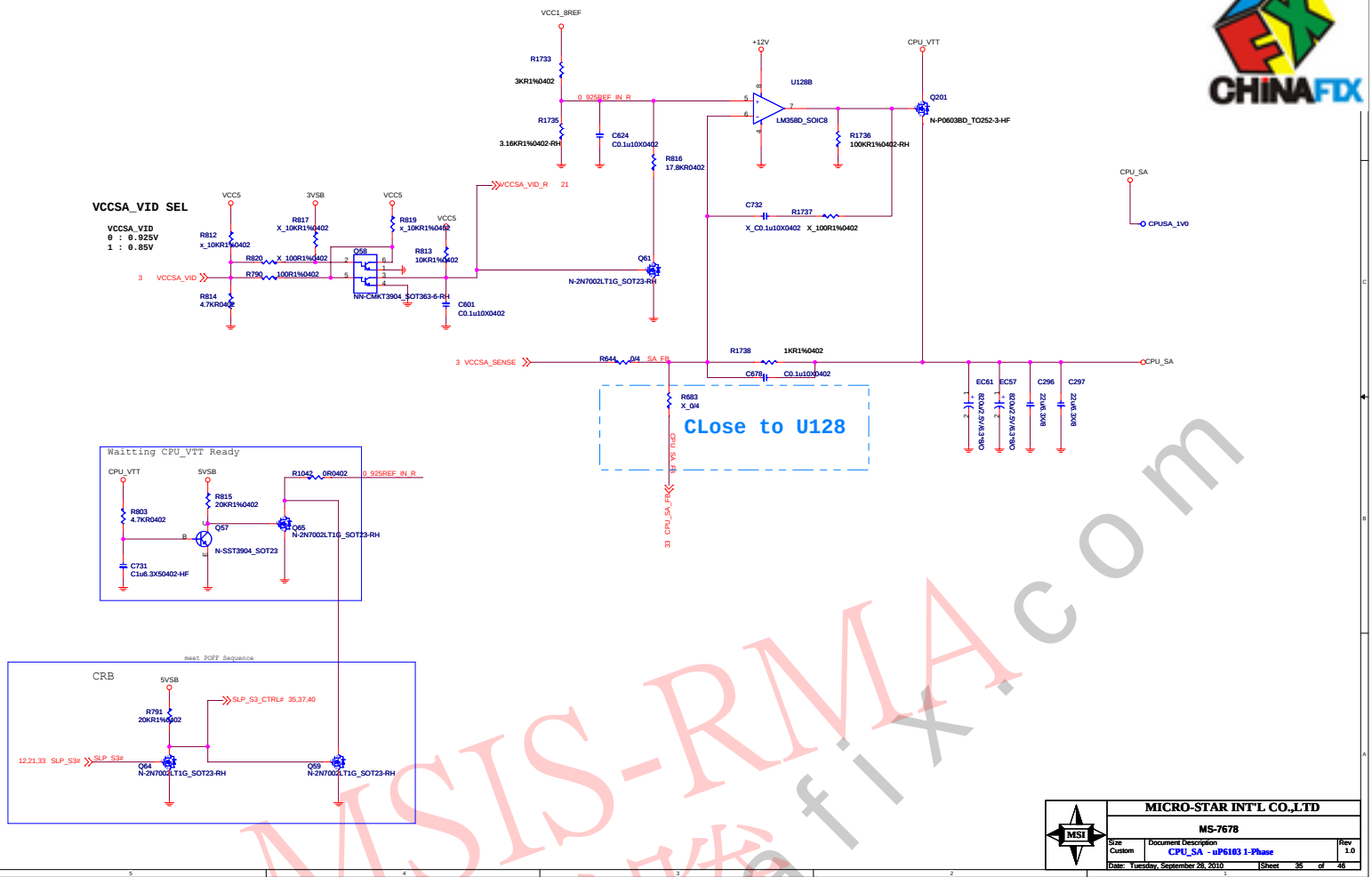
CPU_SA:0.925/0.85

SA Core =8.8A



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Size: Custom	Document Description: CPU_SA - uP6103 1-Phase	Rev: 1.0
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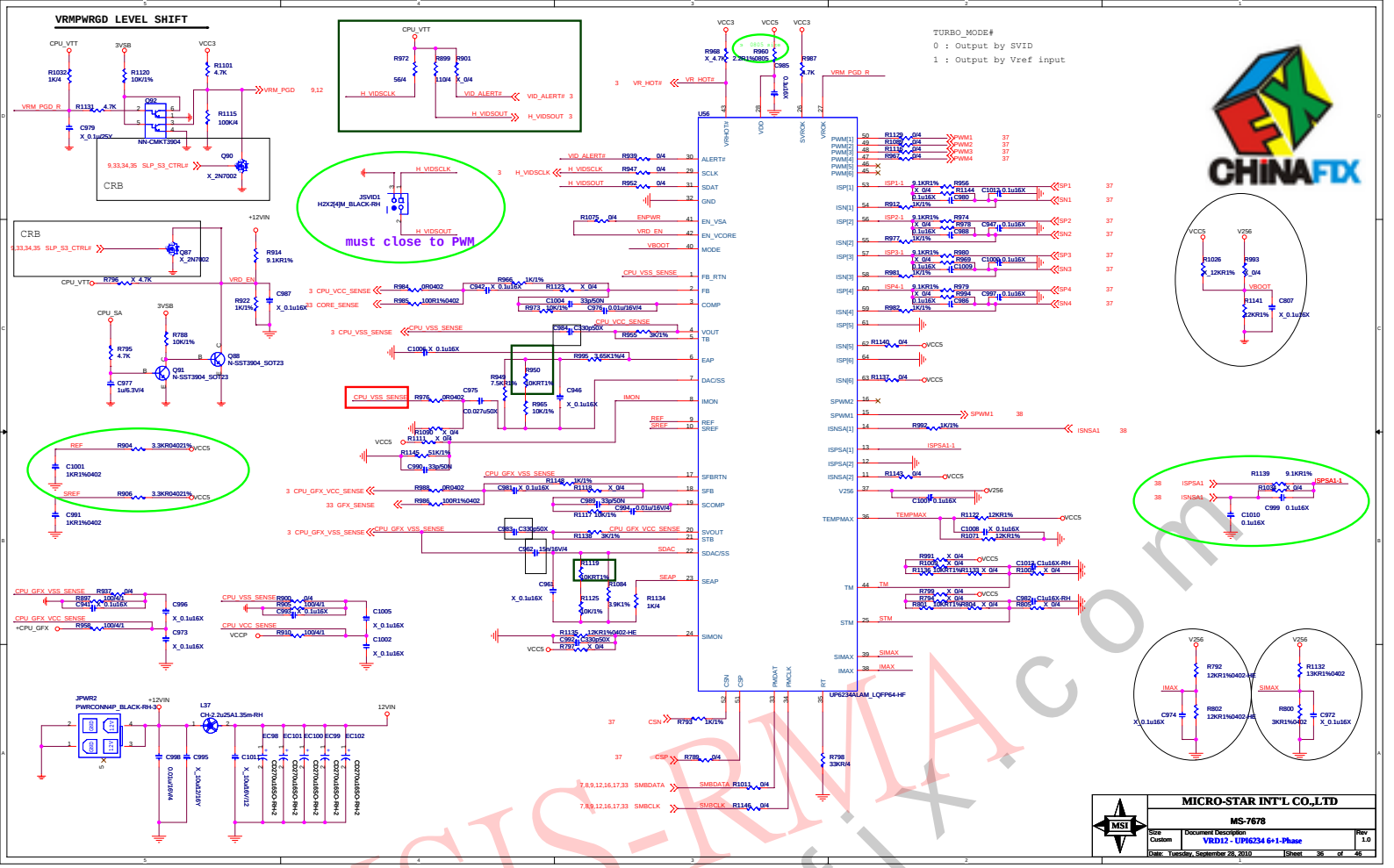

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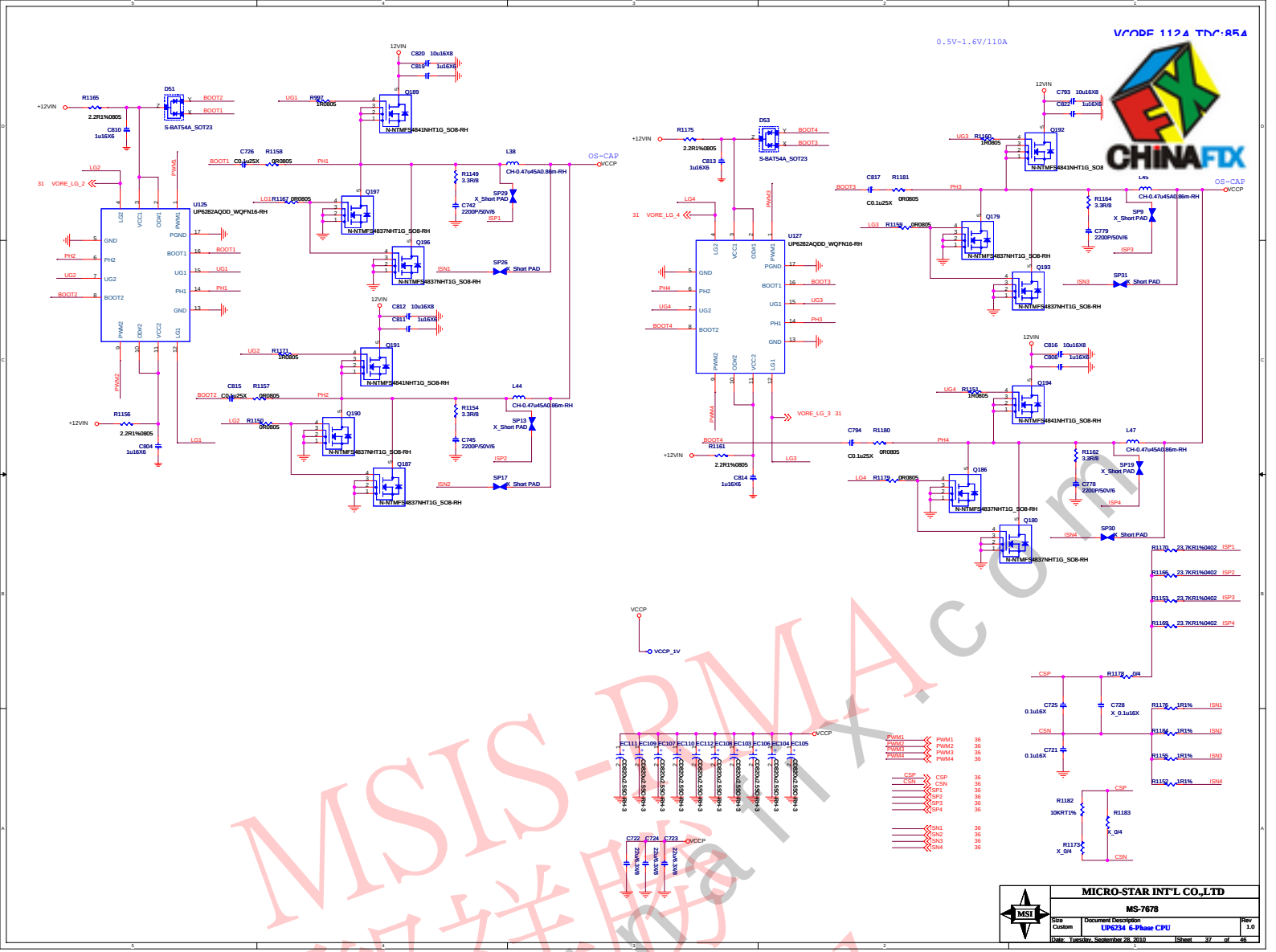

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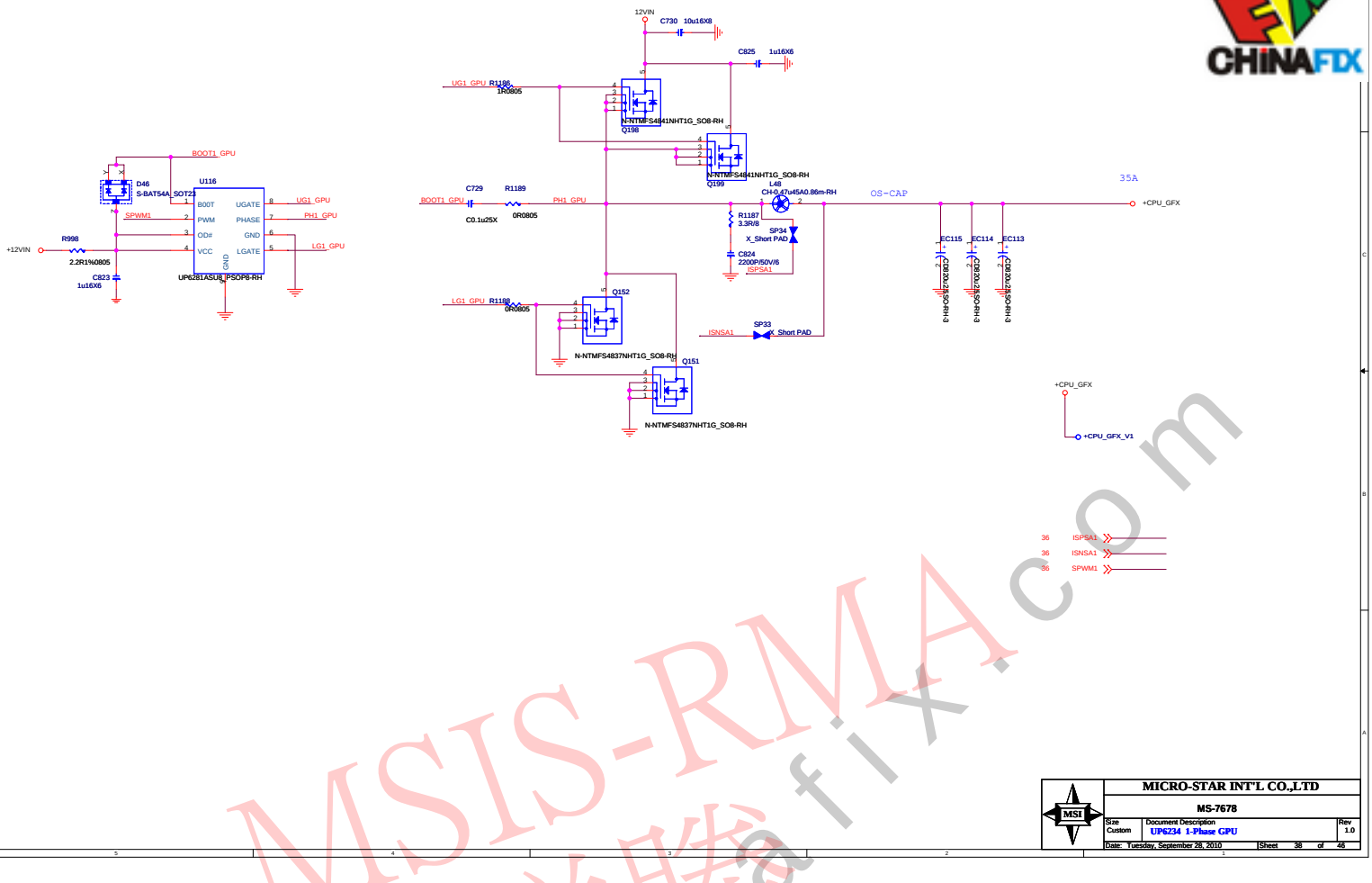

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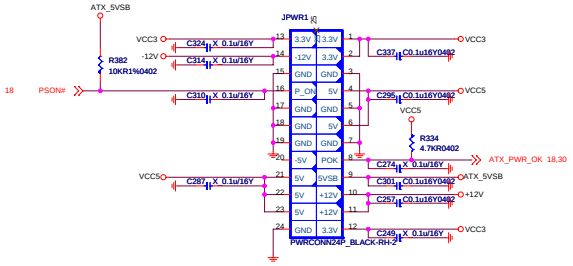
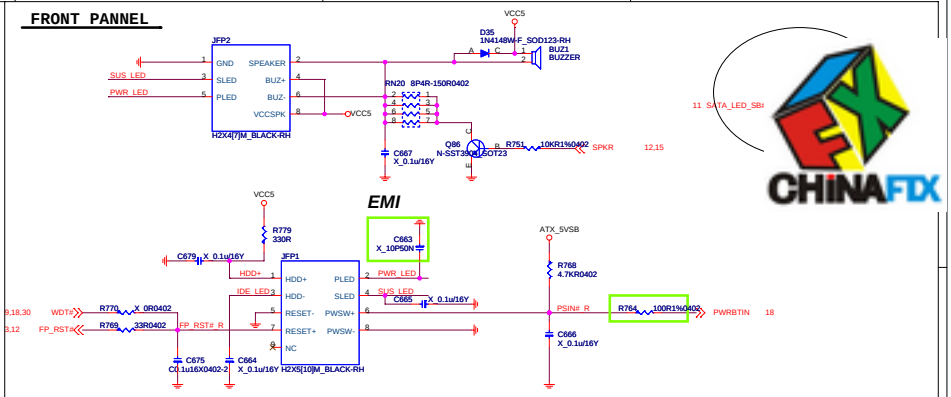
ATX POWER CONNECTOR

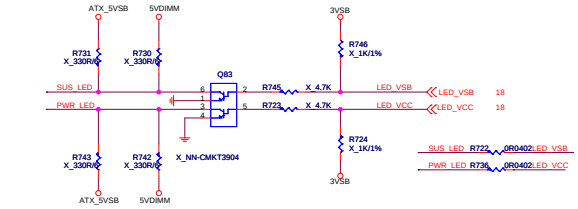


FRONT PANNEL



EMI

LED (for Fintek 71889)



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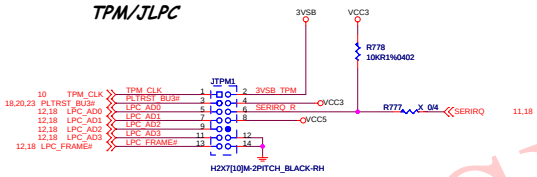

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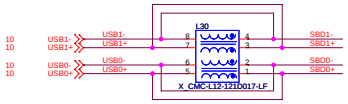
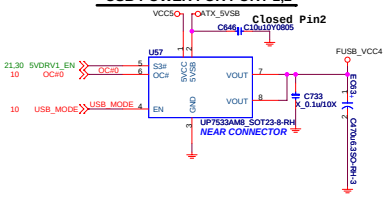
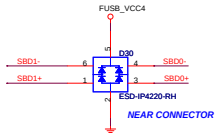
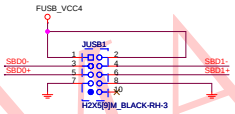
FRONT USB PORT0.1



USB POWER FOR PORT 1,2







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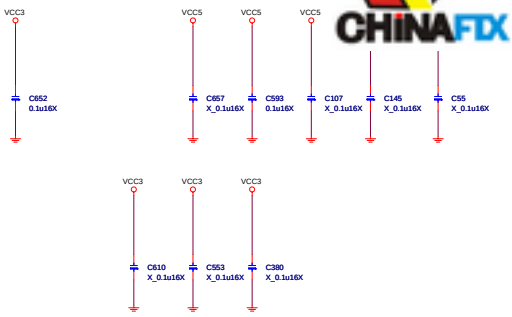
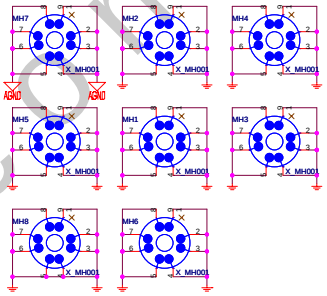
PCH XDP

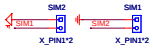


PCH XDP PWRGD/RESET

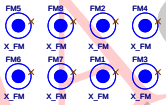
Mounting Holes

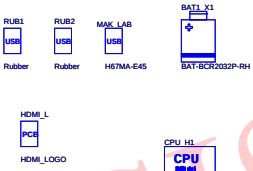


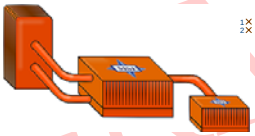
Simulation

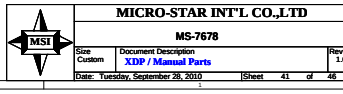


Optical Fiducial Marks-120









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